GOVERNMENT ARTS AND SCIENCE COLLEGE

NAGERCOIL – 629 004

[Affiliated to Manonmaniam Sundaranar University, Tirunelveli – 12]

DEPARTMENT OF PHYSICS

COURSE MATERIAL

NAME OF THE SUBJECT : BASIC ELECTRONICS

SUBJECT CODE : SMPH51

YEAR : III B.Sc. PHYSICS

SEMESTER : V

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SYLLABUS – Manonmaniam Sundaranar University, Tirunelveli – 12

PAPER VII

BASIC ELECTRONICS

Preamble: This course facilitates an understanding of circuit analysis semiconductor diode and transistor circuits and the basics of operational amplifier. The paper does not need any special pre requisite except the basic ideas on Electricity and Electronics at the school level and the learners are expected to gain knowledge to analyse and design electronic circuits

UNIT-I: LINEAR CIRCUIT ANALYSIS Constant voltage source, constant current source, conversion of voltage source into current source - Maximum power transfer theorem - Thevanin's theorem - Norton's theorem - hybrid parameters - determination of h parameter - equivalent circuit - the h parameters of a transistor. (12L)

UNIT-II: SEMICONDUCTOR DIODES AND DEVICES PN Junction - V – I characteristics - Crystal diode as a rectifier - Zener diode - V – I characteristics -Tunnel diode- Half wave rectifier-Centre tap full wave rectifier - Full wave bridge rectifier - Comparison of Rectifiers - Filter Circuits - Types (capacitor filter, choke input filter, Π filter) -Zener diode as voltage stabilizer.
(11L)

UNIT-III: TRANSISTOR AMPLIFIERS Transistor action - Transistor connections - common emitter - common base -common collector - analysis of amplifiers using h- parameters - RC coupled amplifier - transformer coupled amplifier - power amplifier - classification of power amplifiers (Class A, Class B and Class C) – Push pull amplifier - FET charecteristics - JFET characteristics.
(14L)

UNIT-IV: OSCILLATORS AND WAVE SHAPING CIRCUITS
Feedback principle and Barkhaussen criterion - Hartley , Colpitt's, and Phase shift oscillators using transistors – Astable - Monostable and Bistable multi vibrators using transistors - Schmitt trigger - clipping and clamping circuits - Differentiating circuit - Integrating circuit.
(10L)

UNIT-V: OPERATIONAL AMPLIFIER Op-Amp - pin diagram-characteristics of ideal Op - Amp - DC and A.C analysis - bandwidth - slew rate - frequency response - Op- Amp with negative feedback - applications - Inverting amplifier - Non inverting amplifier - Voltage follower- Adder - Subtractor - Integrator – Differentiator- Low pass, High pass and Band pass filters -Wien bridge oscillator.
(13L)

Books for study
1. Principles of Electronics - V.K.Mehta & Rohit Mehta-S.Chand &Co.

Books for reference
1. Electronic fundamentals and applications - John D. Ryder –Prentice Hall
2. Electronic principles - Malvino
3. Electronic devices and circuits - David Bell- Prentice Hall 4. Basic Electronics - B.Basavaraj, H.N.Shivashankar-2 nd edition-University press
5. Physics of semiconductor devices - Dilip K.Roy - University press.

BASIC ELECTRONICS

UNIT-I: LINEAR CIRCUIT ANALYSIS

Constant voltage source, constant current source, conversion of voltage source into current source - Maximum power transfer theorem - Thevanin's theorem - Norton's theorem - hybrid parameters - determination of h parameter - equivalent circuit - the h parameters of a transistor.

CONSTANT VOLTAGE SOURCE

Ideal voltage source (constant voltage source)

A constant voltage source is a power source which provides a constant voltage to a load, even if there happens changes and variance in load resistance.

Consider a source of electric energy such as a lead cell. It may be represented by a voltage source in series with its internal resistance as shown in fig. 4 (The internal resistance may be due to electrolyte in the cell or armature coil in the dynamo). A and B are the terminals of the voltage source.

Let the open circuit voltage = E (without R across AB)
and internal resistance of the source = r

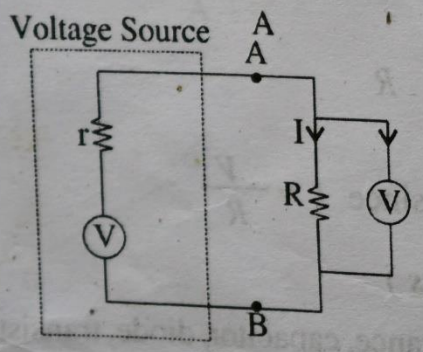


Fig. 4 (a) Ideal voltage source

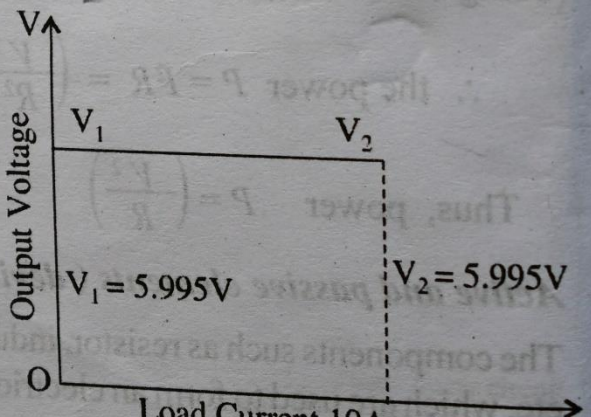


Fig. 4 (b) Characteristics of constant voltage source

Let R be the external resistance (load) connected between A and B. Now the voltage across the load is known as the terminal voltage, V.

The current through the load is $i = \frac{E}{(R+r)}$

The terminal voltage $V = IR = \frac{ER}{(R+r)}$

$$V = \frac{E}{(1+r/R)}$$

If the value of (r/R) is very small compared to 1, the terminal voltage V will be almost equal to the source voltage. When $r = 0$, $V = E$ for any load resistance R. In such a case, the output voltage nearly *remains the same* when load current changes. Such a voltage source is known as an ideal voltage source. Practically r is much less than R.

CONSTANT CURRENT SOURCE

voltage source.

Constant Current Source

A constant current source is a power source which provides a constant current to a load, even if there happens changes and variance in load resistance.

Consider a source of electric energy such as a Daniel cell or a solar cell. It may be represented by a current source (generator) in parallel to its internal resistance, as shown in fig 5. C and D are the terminals for the current source. The symbol for a current source is circle with an arrow inside, showing the direction of the current.

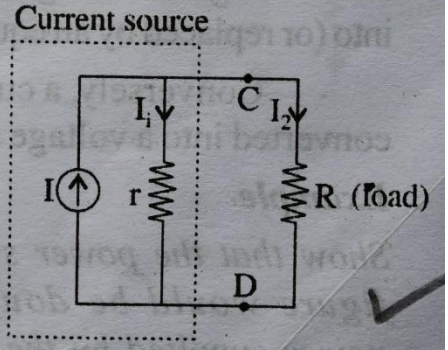


Fig. 5 Constant current source

With $R = 0$. (CD is short circuited), let I be the current supplied by the generator, i.e., I is the short-circuited current. When R is connected between C and D, let I_1 be the current through r and I_2 be the current through R.

We know that $I = I_1 + I_2$ from Kirchoff's law. Also,

potential difference across R = potential difference across r

$$\therefore I_2 R = I_1 r$$

$$\frac{I_1}{I_2} = \frac{R}{r}$$

$$1 + \frac{I_1}{I_2} = 1 + \frac{R}{r}$$

$$\frac{I_1 + I_2}{I_2} = 1 + \frac{R}{r}$$

$$\frac{I}{I_2} = \left(1 + \frac{R}{r}\right)$$

$$I_2 = \frac{I}{(1 + R/r)}$$

If $r = \infty$, the ratio $R/r = 0$. In that case, $I_2 = I$. i.e., the current through the load will be the same as the current produced by the source. The current through the load is *independent* of the load. Such a current source is known as ideal current source. Thus, an ideal current source has infinite internal impedance ($r = \infty$). Practically, r should be much greater than the load resistance R.

Conversion of voltage source into current source

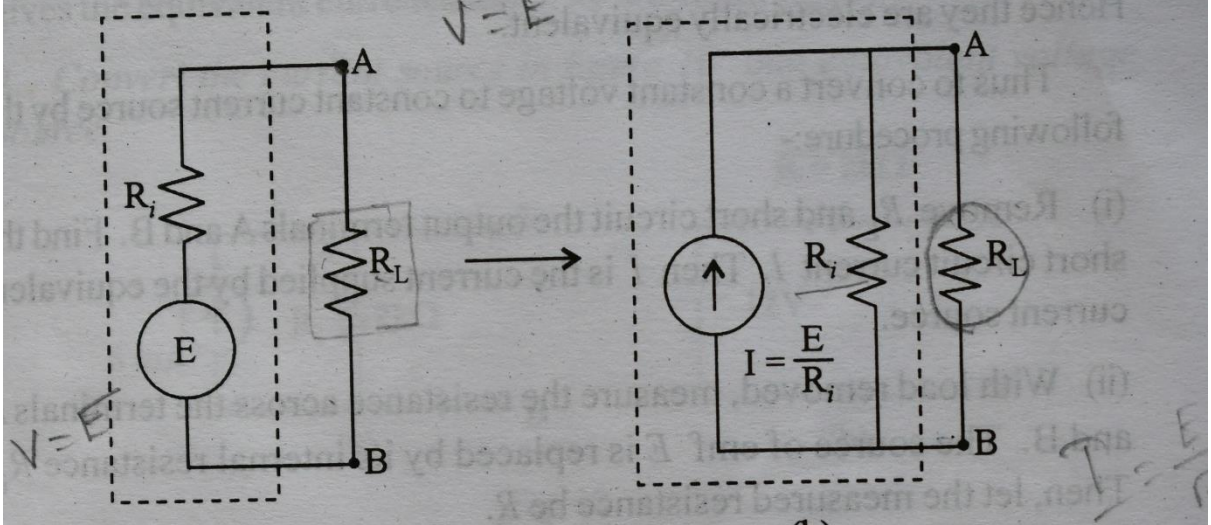


Fig. 8

Source Conversion

A given voltage source with a series resistance can be converted into (or replaced by an equivalent current serice with a parallel resistance.

Conversely, a current source with a parallel resistance can be converted into a voltage source with a series resistance.

MAXIMUM POWER TRANSFER THEOREM

Maximum power transfer theorem

In electronic appliances, a load (loud speaker) is connected across a voltage source (amplifier). Power is transferred from the source to the load. The amount of power transfer depends on the load resistance. Maximum power will be transferred when the load resistance is made equal to the internal resistance of the source. This is known as Maximum power transfer theorem.

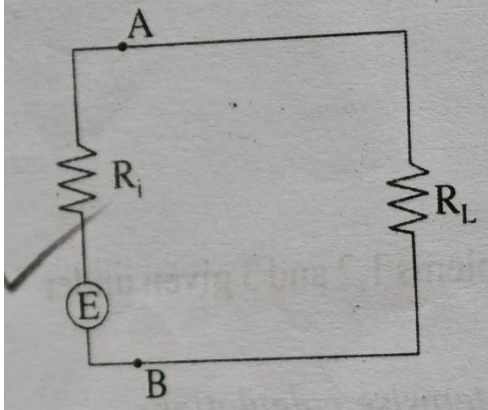


Fig. 37 (a)

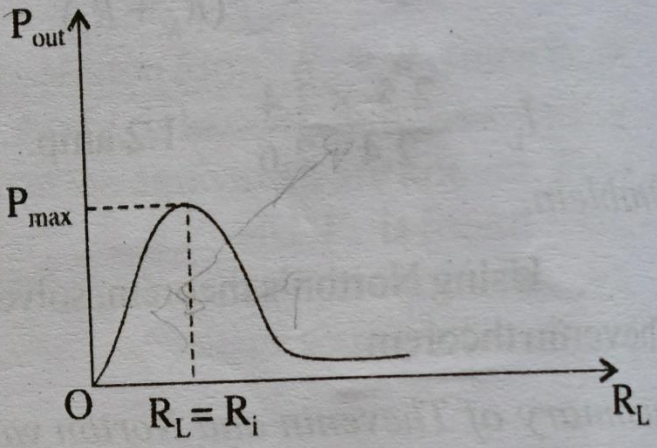


Fig. 37 (b)

The theorem is applicable for both a.c. and d.c circuits since the power is concerned with resistance only. Figure shows a voltage source, generating e.m.f E, having internal resistance R_r Let R_L be the load resistance connected across the voltage source.

The current through the circuit is $I = \dfrac{E}{(Ri + R_L)}$

Power delivered to the load $P = I^2 \times R_L = \left(\dfrac{E}{(R_i + R_L)}\right)^2 \times R_L$

For a given source, the generated voltage E and internal resistance R_i are constants.

$\therefore$ The power (P) delivered to the load depends on R_L.

In order that maximum power is transfered to the load, we have to find $\frac{\partial P}{\partial R_L}$ and put it equal to zero.

$$P = \left(\frac{E}{(R_i + R_L)}\right)^2 \times R_L = \frac{E^2}{(R_i + R_L)^2} R_L$$

$$\frac{dP}{dR_L} = \frac{E^2[(R_i + R_L)^2 . 1 - R_L \times 2(R_i + R_L)]}{(R_i + R_L)^4}$$

$$= \frac{E^2 (R_i + R_L)[(R_i + R_L) - 2R_L]}{(R_i + R_L)^4}$$

$$\frac{dP}{dR_L} = \frac{E^2 (R_i + R_L)(R_i - R_L)}{(R_i + R_L)^4}$$

For maximum power transfer, $\frac{dP}{dR_L} = 0$

$\therefore$ The Nr. of RHS of the above equation is zero. Here E^2 is not zero.

$\therefore (R_i + R_L)(R_i - R_L) = 0$

Since $R_i + R_L$ cannot be zero, we find that, $R_i - R_L = 0$

$\therefore R_i = R_L$

ie, Internal resistance = load resistance.

ie, the load resistance R_L must be equal to the internal resistance of the source. This proves the maximum power transfer theorem.

To calculate the maximum power delivered to the load

$$P = \frac{E^2}{(R_i + R_L)^2} \times R_L$$

Putting $R_i = R_L$, we get the maximum value of P.

$$P_{max} = \frac{E^2}{(R_i + R_L)^2} \times R_L = \frac{E^2}{(2R_L)^2} \times R_L = \frac{E^2}{4R_L}$$

$$= \frac{E^2}{(R_i + R_L)} = \frac{E^2}{2R_L} \qquad \text{Since } R_i = R_L$$

Thus, the power delivered to the load is one half the power generated in the source. The other half power is dissipated in the internal resistance of the source. The efficiency of maximum power transfer is 50 %.

Application

In an amplifier system, maximum power has to be transferred to the speaker from the amplifier. This is achieved by matching the resistance of the loud speaker coil to the output resistance of the amplifier. This principle is known as impedance matching.

When the load is other than pure resistance such as inductance the maximum power will be transfered to the load when the load impedance = conjugate of internal impedance of the generator.

THEVENIN'S THEOREM

Thevenin's Theorem

This theorem helps us to reduce a complicated two-terminal net work to a simple equivalent circuit, containing one voltage source with a series resistance. The theorem is stated as follows:

Any two- terminal net- work containing a number of voltage sources and resistances can be replaced by an equivalent series circuit, having a voltages source V_0 in series with a resistance R_0 connected to the same two terminals. Here V_0 = open circuit voltage between the two terminals (voltage measured with no load between the two terminals) and R_0 = open circuit resistance between the two terminals, with all the sources replaced by their internal resistance (an ohm-meter connected between A and B gives R_0).

Explanation

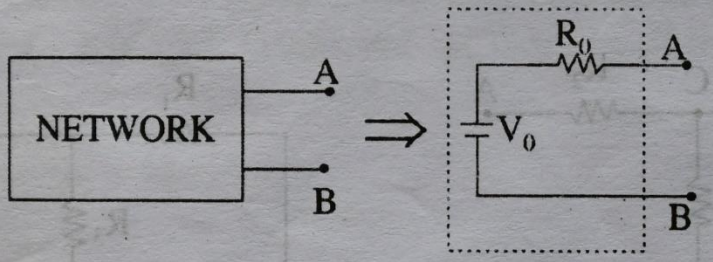
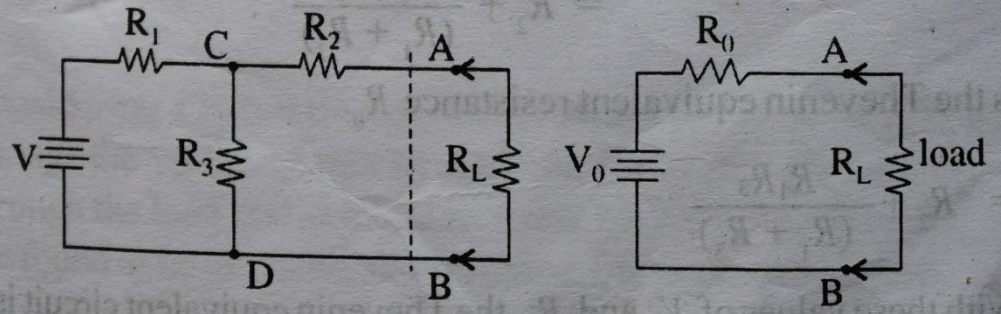


Fig. 8 Thevenin's Theorem

Figure 9 (a) shows a net-work with resistance R_1, R_2 and R_3. A and B are terminals of the network to which the load R_L is connected.. The net work is replaced by an equivalent voltage source V_o in series with the resistance R_0 (fig 9 b).



(a) Given network (b) Thevenin's equivalent circuit

To find V_o

This is the voltage between A and B when the load R_L is removed.

Voltage between A and B = voltage between C and D (Fig.10). Now by potential divider principle, the voltage between C and D = $\frac{V \times R_3}{(R_1 + R_3)}$

This gives the Thevenin voltage V_0.

i.e., $V_o = \frac{V \times R_3}{(R_1 + R_3)}$,

To find R_0

The load R_L is open-circuited (R_L is removed). The voltage source is short-circuited (Fig.11). In this arrangement R_1 and R_3 are parallel to each other.

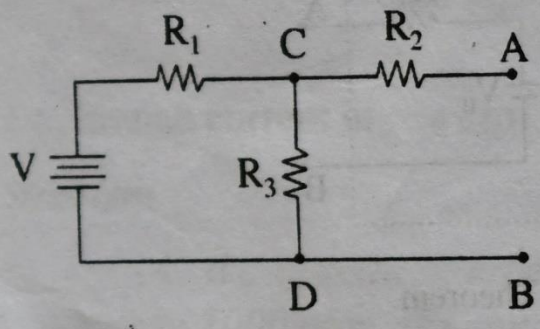


Fig. 10

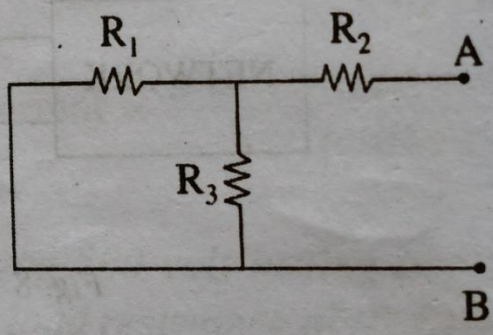


Fig. 11

$\therefore$ Resistance between A and B $= R_2 + (R_1 \,||\, R_3)$

$$= R_2 + \frac{R_1 R_3}{(R_1 + R_3)} \cdot$$

This gives the Thevenin equivalent resistance R_0.

i.e., $R_0 = R_2 + \dfrac{R_1 R_3}{(R_1 + R_3)}$

With these values of V_0 and R_0, the Thevenin equivalent circuit i obtained as shown in fig. 12. The load R_L can now be connected across A and B. The current through the load R_L can be easily obtained as

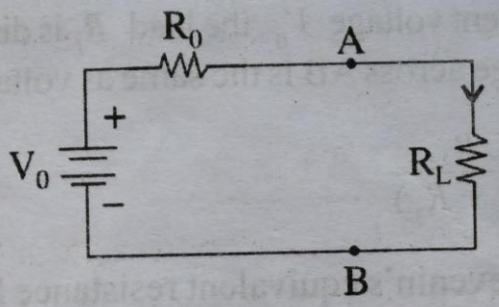


Fig. 12

$$I_L = \frac{V_0}{(R_0 + R_L)} \cdot$$

Once V_0 and R_0 of a given complicated network is determined, the current through any load can easily be calculated using Thevenin's theorem. Also the power delivered to the load resistance R_L can also be found as $P = (I_L^2 R_L)$. This shows the importance of the Thevenin's theorem.

Proof of Thevenin's theorem

Norton's Theorem

The Norton's theorem helps us to reduce a complicated two terminal network to a simple equivalent circuit, containing one current source with a parallel resistance. The theorem is stated as follows:

Any two-terminal net-work containing a number of voltage sources and resistances can be replaced by an equivalent parallel circuit, having a current source (I_N) with a parallel resistance (R_N) connected between the same two terminals.

Here I_N is the short circuited current (with terminals A and B shorted). An ammeter connected between A and B in the network gives I_N. Again R_N is the Norton equivalent resistance with terminals A and B kept open (load resistance R_L is also removed) and when all sources are replaced by their internal resistance. A ohm-meter connected between A and B measures R_N.

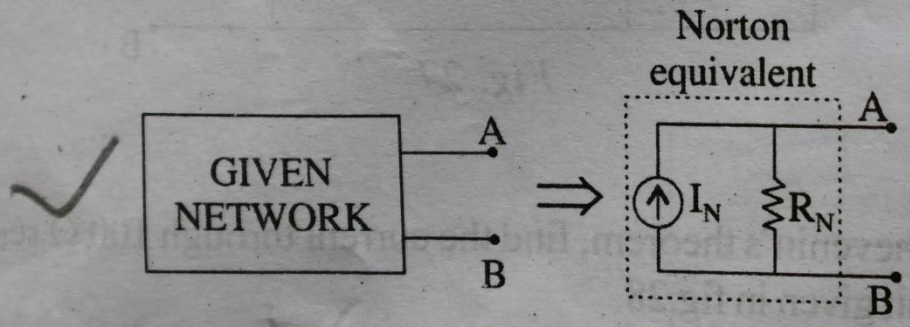


Fig. 29 Norton's theorem

Explanation:

Consider a network consisting of a voltage source (V) and resistance R_1 and R_2, together with a load resistance R_L as in figure 30. With R_L removed, we get a two terminal net work with terminals A and B. Norton theorem enables us to get an equivalent circuit for this.

To find I_N.

The first step is to short-circuit the terminals A and B (fig.31a). The current through the short gives the Norton current I_N. How much is this current? Short-circuiting AB also short circuits R_2. In the remaining circuit, the current flowing is $I_N = (V/R_1)$. This gives the Norton current.

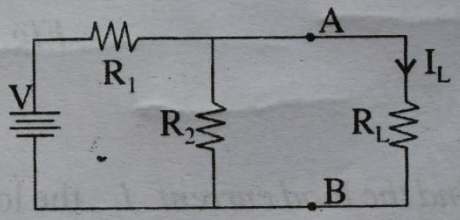


Fig. 30

To find R_N, remove the short-circuit and keep this terminals A and B open, without R_L. The voltage source is shorted (or replaced by its internal resistance, if any).

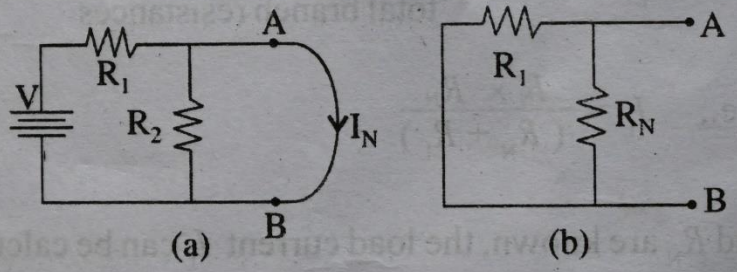


Fig. 31

The resistance appearing between A and B gives the Norton resistance R_N (fig.31 b). In this case,

$$R_N = R_1 \,||\, R_2 = \frac{R_1 R_2}{R_1 + R_2}$$

Since I_N and R_N are known, the Norton equivalent of the given network can be obtained by connecting R_N parallel to the current source I_N. This is shown in the figure 32 (a)

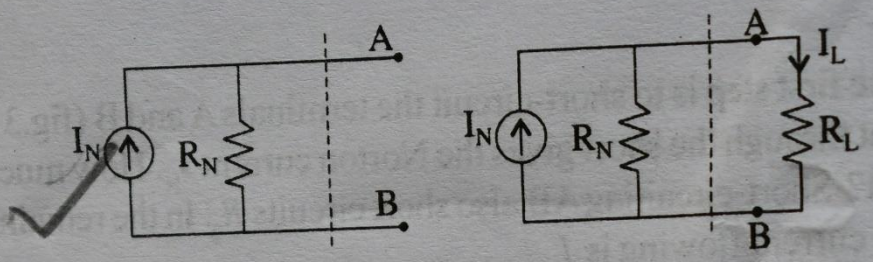


Fig. 32

To find the load current I_L, the load R_L is connected between A and B in the Norton equivalent circuit. The current source delivers current I_N, which divides into two parts through the branches R_N and R_L. The branch current through R_L is given by

$$I_L = \frac{\text{main current} \times \text{other branch resistance}}{\text{total branch resistances}}$$

$$\text{i.e.,} \quad I_L = \frac{I_N \times R_N}{(R_N + R_L)}$$

Since I_N and R_N are known, the load current I_L can be calculated.

Thevenin - Norton conversion (conversion of voltage source into current source)

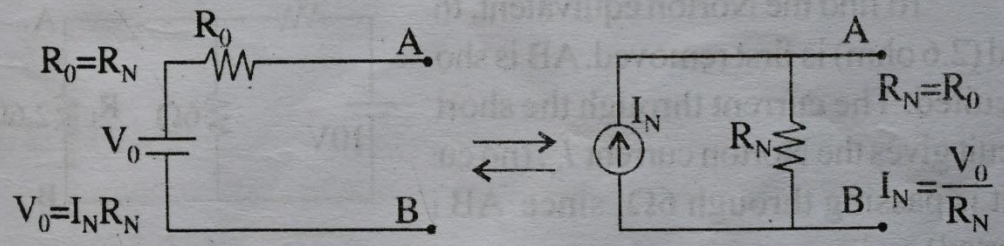


Fig. 34

The Thevenin's theorem says that any network can be represented by a voltage source and a series resistance. Norton theorem says that the same net-work can be represented by a current source and a shunt (parallel) reisistance. Therefore, it must be possible to convert Thevenin equivalent circuit to a Norton equivalent circuit and vice- versa. Figure (34) shows the equivalence between the two.

Let V_o be the Thevenin voltage and R_o be the Thevenin resistance. Let I_N be the Norton current and R_N be the Norton resistance of a given network.

Proceeding from Thevenin to Norton form, $R_N = R_o$ since both are found under the same condition. And I_N is known from the relation $I_N = V_o / R_o$. Thus, R_N and I_N for the Norton equivalent are known. Proceeding from Norton to Thevenin form, $R_o = R_N$ and V_o is found from the relation $V_0 = I_N \cdot R_N$. Thus R_o and V_o for the Thevenin equivalent are known. This also illustrates the conversion of voltage source into current source and vice-versa.

Process	Thevenin	Norton
Step 1.	Open the load resistor	Short-circuit the load resistor
Step 2.	Calculate (or measure) the open circuit voltage. This is Thevenin voltage, V_o	Calculate (or measure) the short circuit current. This is Norton current, I_N
Step 3.	Short circuit voltage sources and open current sources and open load resistor	Short circuit voltage sources; open current sources;and open load resistor.
Step 4.	Calculate (or measure) the open circuit resistance. This is Thevenin resistance R_o.	Calculate (or measure) the open circuit resistance. This is the Norton resistance, R_N. $V_o = I_N R_N$

HYBRID PARAMETERS AND DETERMINATION OF H PARAMETER

Two port net-work and h-parameter equivalent circuit

In many electronic systems, there are four terminals: two for the input and two for the output.

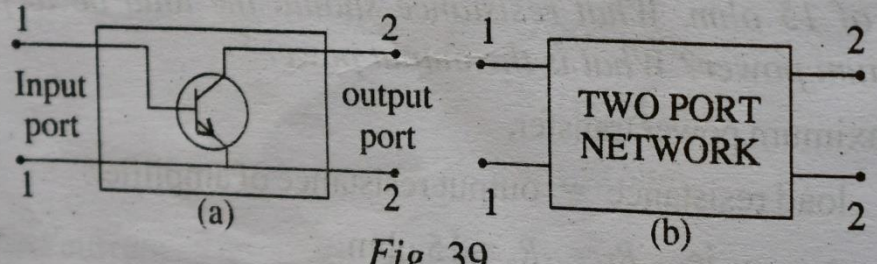


Fig. 39

The quantities within the brackets are represented by h symbol with different suffix.

i.e., $v_1 = h_{11} i_1 + h_{12} v_2$ ..... (1)

and $i_2 = h_{21} i_1 + h_{22} v_2$. ..... (2)

when $v_2 = 0$ in equation (1), $h_{11} = \left(\frac{v_1}{i_1}\right)$. The coefficent

$h_{11} = \left(\frac{v_1}{i_1}\right)_{v_2=0}$ This ratio is called the input impedance h_i (with output shorted)

i.e., $h_{11} = h_i$

Now, when $i_1 = 0$, $h_{12} = \left(\frac{v_1}{v_2}\right)$. from equation (1)

The coefficient $h_{12} = \left(\frac{v_1}{v_2}\right) i_1 = 0$ This ratio is called the reverse voltage transfer ratio, h_r. (with open circuited)

i.e., $h_{12} = h_r$

Again, when $v_2 = 0$ in equation (2), we have $h_{21} = \frac{i_2}{i_1}$.

The coefficient $h_{21} = \left(\frac{i_2}{i_1}\right)_{v_2=0}$ This ratio is called the forward current gain, h_f (with output shorted).

i.e., $h_{21} = h_f$

Also, when $i_1 = 0$ in equation (2), we have $h_{22} = \frac{i_2}{v_2}$. The coefficient $h_{22} = \left(\frac{i_2}{v_2}\right)_{i_1=0}$ This ratio is called the output admittance, h_o (with input open circuited).

i.e., $h_{22} = h_o$

Why hybrid parameter equivalent ciruits are widely used?

1. The *h* - parameters can be measured easily.
2. They are more independent of each other and other variables like frequency and operating point.
3. The value of *h* - parameters nearly corresponds to the actual values of input and output impedances and the current gain (of the net work) for many applications.
4. The *h* - parameters are real numbers at audio frequencies.
5. The *h* parameter equivalent circuits are particularly suitable for circuit analysis and design and are commonly specified by transistor manufactures.

EQUIVALENT CIRCUIT - THE H PARAMETERS OF A TRANSISTOR.

Transistor h parameters and their Experimental determination

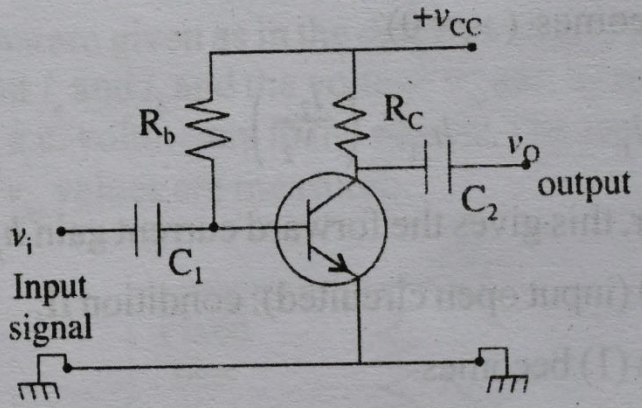
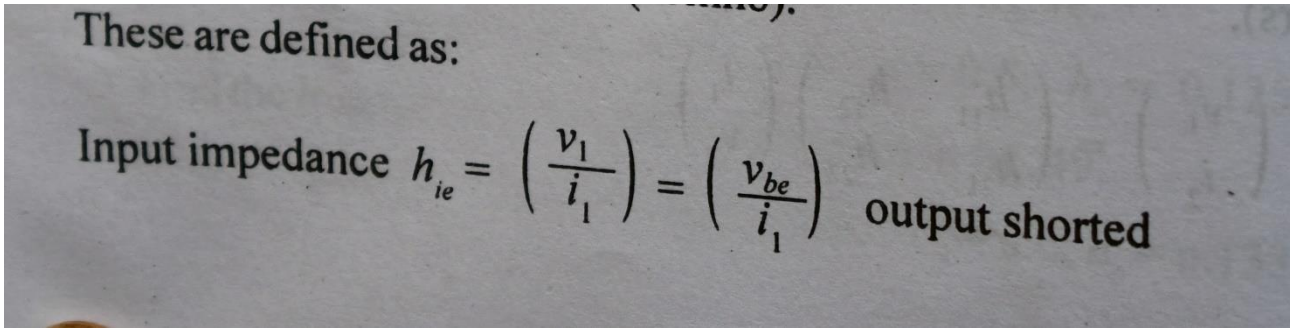
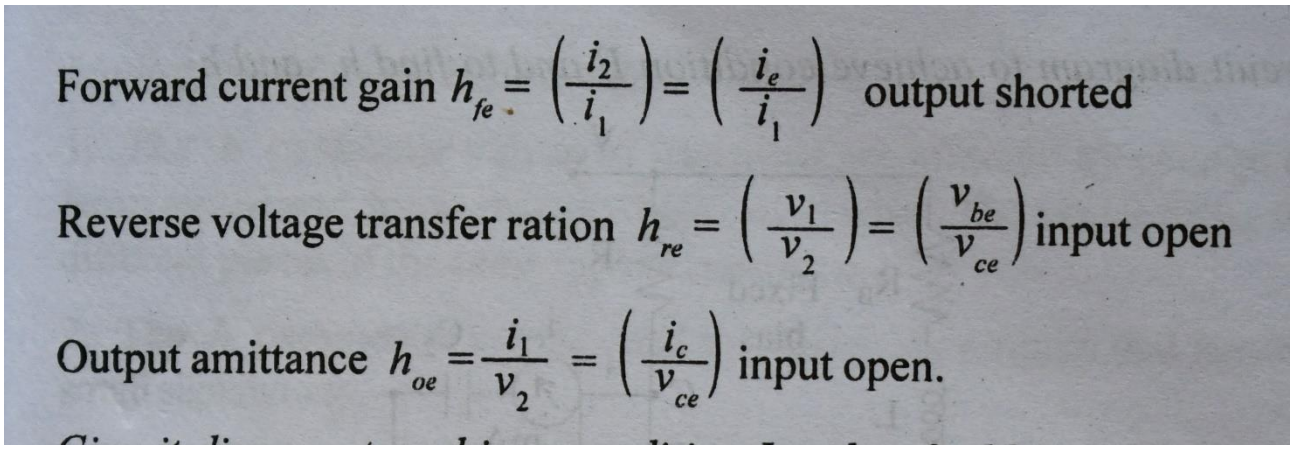


Fig. 50 Transistor amplifier

Figure 50 shows a transistor connected in the common emitter mode. The transistor *h* parameters for common emitter mode (CE mode) are h_{ie} (input impedance), h_{fe} (forward current gain), h_{re} (reverse voltage transfer ratio and h_{oe} (the output admittance). The first two parameters can be found out, by keeping output (of the CE amplifier circuit) shorted. The last two parameters can be found out by keeping the input (of the amplifier circuit) open. The circuits are made up accordingly.

Definition





QUESTIONS FROM PREVIOUS YEAR QUESTION PAPERS

PART A

In a p-type semiconductor the majority carriers are ————— and the minority carriers are —————.

(a) Ions, holes (b) Holes, ions (c) Holes, free electrons (d) Free electrons, holes

A pentavalent impurity has ————— valence electrons.

(a) 4 (b) 5 (c) 6 d) 3

The interval resistance of a constant current source is

(a) small (b) large (c) zero (d) infinite

When a pentavalent impurity is added to intrinsic semiconductor it becomes

(a) an insulator (b) pure semi conductor (c) p-type semiconductor (d) n-type semiconductor

If the temperature changes, h-parameters of a transistor

(a) may or may not change (b) do not change (c) also change (d) none of the above

Thevenin's theorem reduces a two terminal network to a

(a) Constant current source with parallel impedance (b) Constant voltage source with a series impedance (c) One terminal network (d) Constant voltage source in parallel with a high impedance

'Diode' belongs to the class of —————— device

(a) Active (b) Passive (c) Hyperactive (d) None of these.

The band gap of Ge ~ —————— Ev

(a) 0.8 (b) 0.5 (c) 0.6 (d) 0.7.

In a p-type semiconductor the majority carriers are ————— and the minority carriers are —————.

(a) Ions, holes (b) Holes, ions (c) Holes, free electrons (d) Free electrons, holes

A trivalent impurity has ————— valence electrons.

(a) 4 (b) 5 (c) 6 (d) 3

The output current of an ideal current source is
(a) zero (b) constant (c) dependent on load resistance (d) dependent on internal resistance

To get the Thevenin's voltage , you have to
(a) short the load resistor (b) open the load resistor (c) short the voltage source (d) open the voltage source

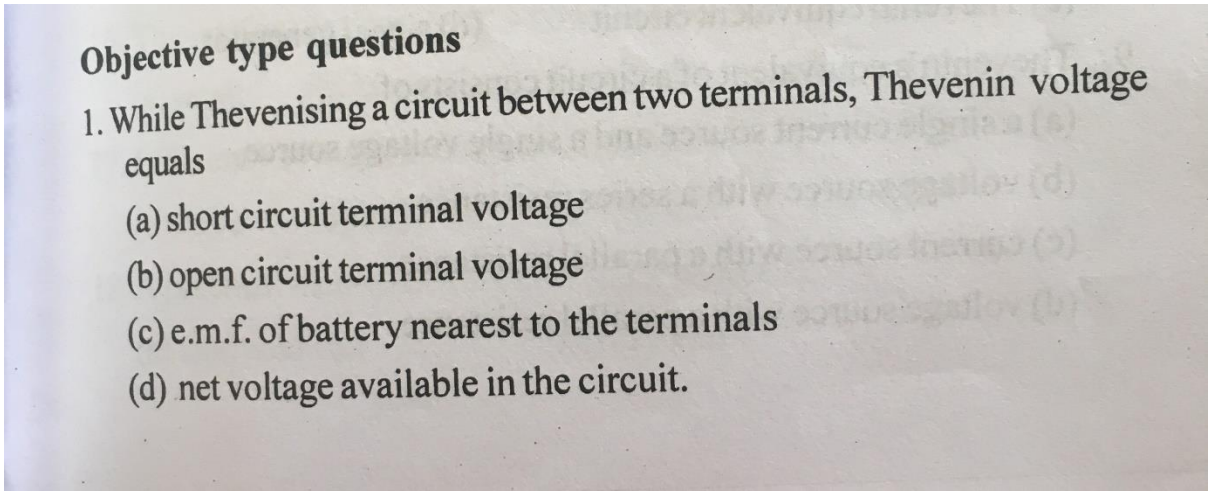
PART B

Explain constant voltage source.
Discuss the effect of temperature in semiconductors.
Explain the concept of a voltage source.
What do you understand by hybrid parameters? What are their dimensions?
Explain Nortons theorem
What are intrinsic semiconductors? Explain briefly.
What are the significant properties of semiconductor materials? Give two examples for Semiconductors.
Distinguish between intrinsic and extrinsic semiconductors
State and explain maximum power transfer theorem.

PART C

State and prove Thevenin's theorem.
Describe the formation of N and P type semiconductor.
State and explain Norton's theorem. How is Norton's equivalent circuit related with the Thevenin's equivalent circuit?
What do you mean by the h-parameters of a transistor? Give their nomenclature.
Discuss the transistor circuit performance in h-parameters.
Explain V-I characteristics of a diode
State and prove Thevenin's theorem.
Explain the working of the junction diode and discuss its V-I characteristics.
What is meant by n-type and p-type semiconductors? Explain with neat diagrams
State and explain Thevenin's theorem and Norton's theorem.
Explain constant current source. How will you convert voltage source into current source?

QUESTIONS FROM BOOK



Objective type questions

1. While Thevenising a circuit between two terminals, Thevenin voltage equals
(a) short circuit terminal voltage
(b) open circuit terminal voltage
(c) e.m.f. of battery nearest to the terminals
(d) net voltage available in the circuit.

2. The Norton equivalent of a circuit consists of a 2 A current source in parallel with 4 Ω resistor. The Thevenin equivalent of this circuit will have a source voltage of ..... in series with 4 Ω resistor.

(a) 2 V (b) 0.5 V (c) V (d) 8 V

3. The unit of output admittance of two-port net work is

(a) ohm (b) henry (c) ampere (c) mho

4. The input impedance of a two port net work is measured with

(a) input open (b) output open

(c) output shorted (d) input shorted

5. In a two-port net work, the ratio of change of input voltage to the change of input currents with output shorted, is called

(a) forward current gain (b) input impedance

(c) output admittance (d) short circuit gain

6. In the two port network with V_1, I_1 and V_2, I_2 as input voltage, input current and output voltage, output current respectively, the independent variable chosen to obtain hybrid parameters of the net work are

(a) I_1, V_2 b) I_1, V_1 c) I_2, V_2 (d) I_2, V_1

7. Of the four h- parameter, the one with the unit mho is

(a) output admittance (b) output impedance

(c) input impedance (d) reverse voltage transfer ratio

8. In the *h*-parameter equivalent circuit or a two port netwosrk, the input port can be represented by

(a) Norton equivalent circuit (b) amplifer circuit

(c) Thevenin equivalent circuit (d) signal generator

9. Thevenin's equivalent of a circuit consists of

(a) a single current source and a single voltage source

(b) voltage source with a series resistance

(c) current source with a parallel resistance

(d) voltage source with a parallel resistance

10. Norton's equivalent of a circuit consists of

(a) ideal voltage source and a parallel resistor

(b) ideal current source and a parallel resistor

(c) ideal voltage source and a series resistor

(d) ideal current source and a series resistor

11. Thevenin's theorem can be applied to

(a) d.c.circuits only (b) a.c. circuits only

(c) both d.c. and a.c. circuits (d) none of the above

12. In the *h*-parameter equivalent circuit of a two port net work, the output port can be represented by

(a) amplifier circuit (b) singal generator

(c) Norton equivalent (d) Thevenin equivalent circuit

13. Open circuit voltage is the p.d. between two points, having

(a) zero impedance (b) finite impedance

(c) infinite impedance (d) reactive impedance

14. Short -circuit current flows through a load of

(a) infinite impedance (b) zero impedance

(c) capacitive impedance (d) inductive impedance

15. The internal resistance of an ideal voltage source is

(a) small (b) large (c) infinite (d) zero

16. The internal resistance of a constant current source is

(a) small (b) large (c) infinite (d) zero

17. Efficiency at maximum power transfer is

(a) 75% (b) 25% (c) 90% (d) 50%

18. A practical example of ideal voltage source is

(a) lead acid cell (b) dry cell

(c) Daniel cell (d) none of the above

19. To get Thevenin voltage, we have to

(a) short circuit load resistor (b) open circuit load resistor

(c) short the voltage source (d) open the voltage source

20. To get the Norton current, we have to

(a) short the load resistor (b) open the load resistor

(c) short the voltage source (d) open the voltage source

21. Under the condition of maximum power transfer a voltage source is delivering a power of 30 W to the load. The power generated by the source is

(a) 45W (b) 60W (c) 30W (d) 90W

22. The *h* parameters of a transistor

(a) are constants at all temperatures

(b) vary with temperature

(c) are high at high temperatures and low at low temperatures

(d) none of the above.

23. Which of the *h* - parameters has the highest value?

a) h_{ie} (b) h_{fe} (c) h_{re} (d) h_{oe}.

24. Which of the *h* - parameters has the lowest value?

(a) h_{ie} (b) h_{fe} (c) h_{re} (d) h_{oe}

Answers

1.(b)	2. (d)	3. (d)	4. (c)	5. (b)	6. (a)	7. (a)
8. (c)	9.(b)	10. (b)	11. (c)	12. (c)	13.(c)	14. (b)
15. (d)	16. (c)	17. (d)	18. (a)	19.(b)	20. (a)	21. (b)
22. (b)	23. (a)	24. (d)				

Questions

1. Explain 'constant voltage source' and ' constant current source', with one example for each. Also explain conversion of voltage source into a current source. What are the practical applications of a constant current source?

2. State and prove maximum power transfer theorem. Give one example for application of maximum power transfer theorem. Why is maximum power transfer theorem important in electronic circuits?

3. State and prove Thevenin's theorem.

4. State and explain Norton's theorem.

5. Show that the maximum power that can be delivered to the load is one half the power generated in the network, driving the load.

6. Explain how it is possible to convert Thevinin equivalent circuit into Norton equivalent circuit and vice-versa.

7. Define hybrid parameters of a linear circuit. Explain how *h*-parameter equivalent circuit can be drawn.

8. Explain, with the help of *h* - parameter equivalent circuit, the performance of a linear circuit in terms of the parameters. Obtain expression for (i) input impedance (ii) current gain and (iii) voltage gain of the linear circuit.

9. Define *h* parameters of a transistor. Explain, giving *h* parameter equivalent circuit, the performance of a transistor circuit in common emmitter mode. Obtain expression for (i) input impedance (ii) current gain (iii) voltage gtain (iv) power gain and (v) output admittance of the transistor circuit.

10. Define *h* parameters of a transistor in CE mode. Describe, giving necessary circuit diagrams, the experimental determination of *h* parameters of a transistor.

UNIT-II

SEMICONDUCTOR DIODES AND DEVICES

PN Junction - V – I characteristics - Crystal diode as a rectifier - Zener diode - V – I characteristics -Tunnel diode- Half wave rectifier-Centre tap full wave rectifier - Full wave bridge rectifier - Comparison of Rectifiers - Filter Circuits - Types (capacitor filter, choke input filter, Π filter) -Zener diode as voltage stabilizer.

p-n- junction

When a *p*-type semiconductor is grown over an *n*-type semiconductor as one crystal so that the lattice is continuous, a *p-n* junction is formed. The region (area) where the *p*- and *n*-type materials physically join is called a *p-n* junction. Having *p*- and *n*-type material merely in contact is not enough. The device is called p-n junction diode with A as the anode and C as the cathode.

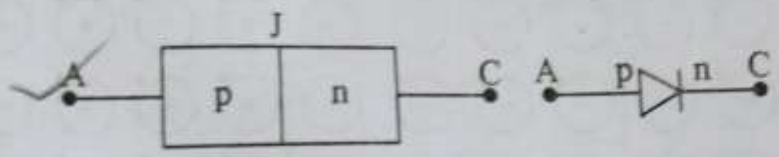


Fig. 57 P-n junction diode.

The diode is symbolically represented by an arrow head (*p*) meeting a bar (*n*). The arrow head shows the direction of the current flow in the diode.

The electrons in the *n*-region have higher concentration than the electrons in the *p* region. So the electrons diffuse across the junction *J* towards the *p* region, where holes are the majority carriers. As soon as the electrons reach the *p* region, the holes and electrons recombine, leaving an excess negative ions there. The negative ions in the *p* region, oppose further diffusion of electrons from the *n*-side. Similarly holes from *p*-type diffuse into the *n* type to be filled by the electrons there and static positive ions remain in the *n* type region.

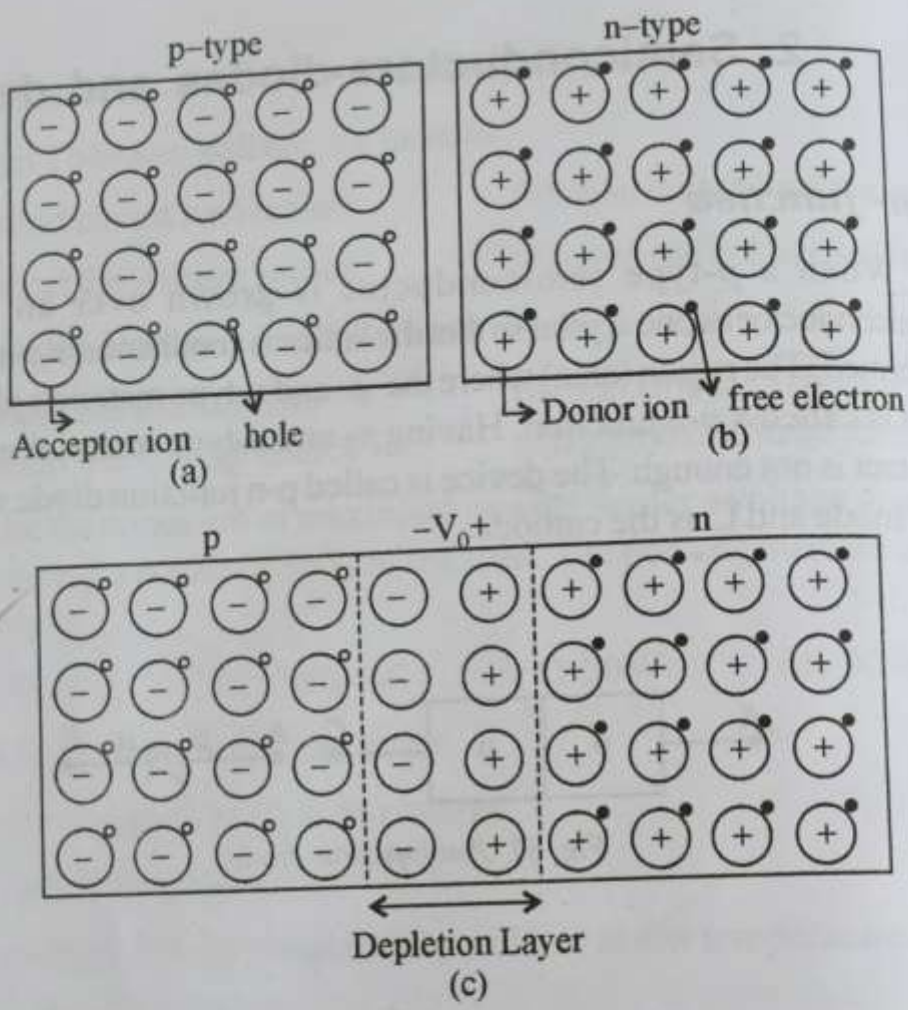


Fig. 58 Formation of Depletion region and built - in - potential of p-n junction.

When the diffusion of electrons stops (during equilibrium), an opposing p.d. is set up across the very narrow layer at the junction by the fixed positive and negative ion on either side. This narrow region near the junction is depleted of free mobile charges *i.e.*, this region is free from mobile charges. Hence this charge-empty region is called the *depletion region* and the p.d. across the depletion region is known as the *built-in potential* V_o. The value of V_o is about 0.3 volt for Ge diodes and 0.7 volt for Si diodes (Fig.). The width of the depletion region is one micron (1×10^{-6}m) normally. The barrier potential cannot be measured

The built-in potential is equivalent to a potential hill or potential barrier to the movement of electrons from the *n* region to the *p* region. Since this potential stops additional electrons from crossing the junction from *n* side to *p* side, the potential is barrier potential. With the depletion region near the *p-n* junction, the crystal will behave like an insulator.

Thus to push electrons from *n*-region to *p*-region further, energy has to be supplied by applying suitable external d.c. voltage, known as bias voltage.

V-I Characteristics of P-N Junction

Biasing a p-n junction: Forward bias

An external battery is connected across the junction with its positive terminal to the *p*-side of the diode and its negative terminal to the *n*-side of the diode. This kind of biasing is known as forward biasing of the junction. (*P* to *p* and *N* to *n*).

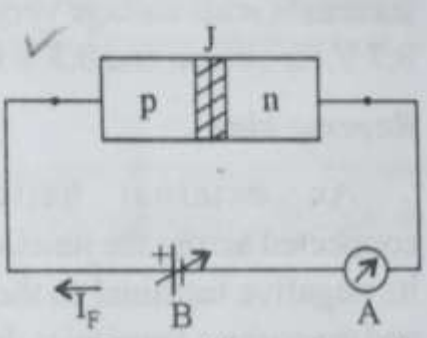


Fig. 59 Forward bias of p-n diode

The positive potential of the battery repels the holes on the *p*-side and pushes them towards the junction *J*. The negative potential of the battery repels the electrons on the n-side and pushes them towards the junction. This collapses (tends to narrow down) the depletion region.

Thus, when forward bias (a potential *V*) is applied across the junction, the barrier is reduced. So more electrons move from *n* side to the *p* side. Therefore an electric current flows across the *p-n* junction. The current is in the direction from *p* to *n* side. This current is known as the forward current and it is of the order of milliamperes. When the applied voltages *V* is increased, the forward current *I* through the diode also increases.

In the low current region, the external bias is used to overcome only the potential barrier (0.3 V for Ge and 0.7 V for Si). The voltage drop due to the ohmic resistance of the semiconducting material is negligibly small in the region. In the high current region, the external bias is used to overcome only ohmic resistance of the semiconducting material. Hence the material behaves as an ordinary conductor (resistance wire) and the current increases with voltage very sharply. The curve is almost linear beyond 0.7 V for silicon and 0.3 V for germanium.

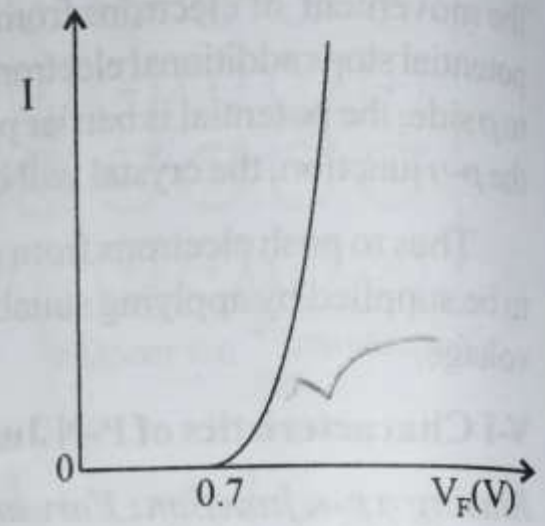


Fig. 60 ' Forward bias Characteristics

Reverse bias

An external battery is connected across the junction with its negative terminal to the *p* side and the positive terminal to the *n* side of the diode. This kind of biasing is known as the 'reverse biasing' of the junction (*P* to *n* and *N* to *p*).

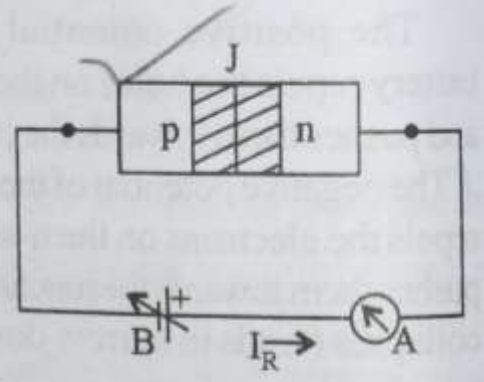


Fig. 61 *Reverse bias of p-n diode*

This arrangement attracts the electrons away from the juction in the n region. Similarly the negative terminal of the battery attracts the holes away from the junction *J* in the *p* - region. This makes the depletion region wider.

As a result of reverse biasing, the potential hill height is increased and hence the junction resistance becomes very high for the movement of holes and electrons across the junction and no appreciable current flows through the junction.

However, in actual practice, under reverse bias there is a feeble current through the diode from n-side. *p*-side. The current is due to movement of minority carriers in the *p* and n regions, crossing the junction. This current is known as reverse current, as the bias is now the reverse bias. The reverse current is of the order of micro ampere. When the reverse bias is increased the current reaches a small maximum value. The current remains constant for further increase of reverse voltage (fig.). The maximum value of current reached under reverse bias is known the *reverse saturation current* I_0.

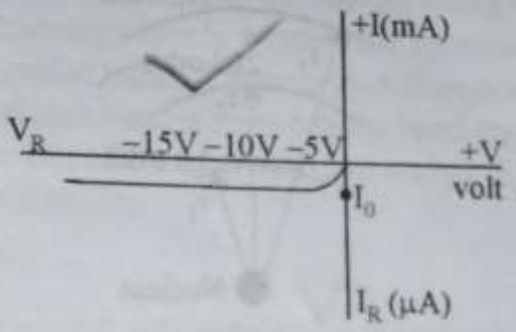


*Fig.*62 *Reverse bias saturadtion current: Reverse bias characterists*

The reverse saturation current I_0 is a measure of the minority carriers crossing the junction and it depends only on the temperature of the diode. It doubles for each 10°C rise of temperature.

Experiment to study the volt-ampere characteristics of a *p-n* junction diode

The *p-n* diode is forward biased by connecting the *p* terminal to the positive side of the battery and *n* terminal to the negative side of the battery. The voltage *V* applied across the diode can be varied using a rheostat and the voltage can be measured using a voltmeter, V and the current *I* through the diode using a milliammeter (Am). To prevent very large current flowing through the diode, a safety resistance *R* is included in the circuit.

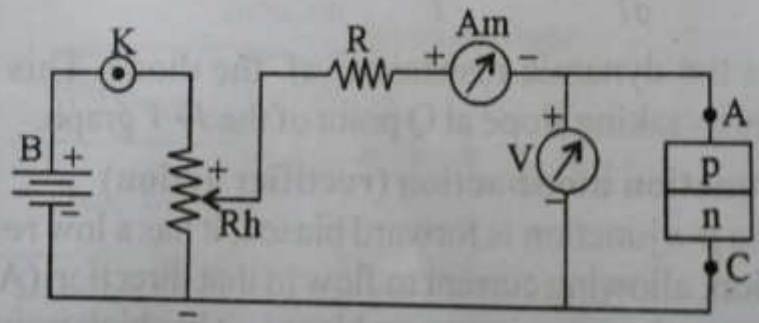


Fig. 69 Experiment to study the volt - ampere characteristics of a p-n junction diode.

The key K is switched on. Starting from zero voltage, the milliammeter readings (*I*) are noted for various voltmeter readings (*V*). The polarity of the battery is reversed such that the diode is reverse biased.

The ammeter readings (μA) for various voltmeter readings are noted. A graph is drawn taking voltage along the X-axis and the corresponding current along the Y-axis. The curve is as shown in the graph. The curve is known as the *I-V* characteristics of the diode.

The portion OQP of the graph is known as the forward bias characteristics of the diode. The portion OR is the reverse bias characteristics of the diode.

(i) *To find the knee voltage:* When the diode is forward biased, the

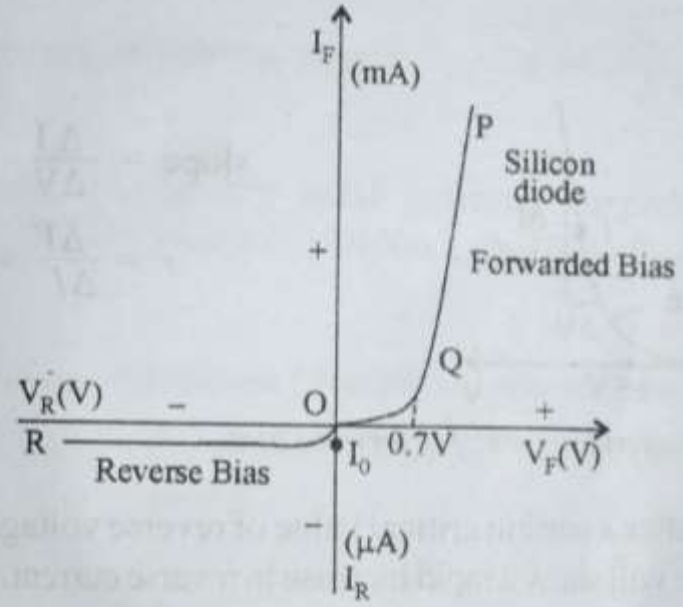


Fig. 70 V-I Characteristic curve for a diode.

current varies with the voltage very slowly in the low current region. The variation is rapid in the high current region. The voltage at which the current starts to increase rapidly is known as the *knee voltage* of the diode. (0.7 V for silicon diode and 0.3 V for germanium diode). This can be found by extrapolating the graph from the linear portion to meet the voltage axis.

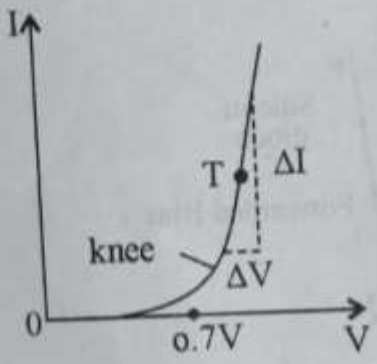
(ii) *To find the a.c. forward resistance of the diode*

The ratio of the *change* in voltage across the diode to the resulting *change* in current through the diode is known as the forward resistance

of the diode. To find this, the slope of the I-V graph at a point T on the linear portion is measured. The a.c. forward resistance $r = \frac{1}{\text{slope}}$ can be calculated.

(iii) *To find the reverse saturation current, I_o*

In the *I-V* graph for reverse bias, we find that the current increases with voltage and soon reaches a maximum value. It remains constant for any further increase of voltage. The constant current can be read in the negative Y axis of the graph as I_o. This gives the reverse saturation current of the diode at the room temperature ($I_o = 5$ nA for silicon).



$$\text{slope} = \frac{\Delta I}{\Delta V}$$

$$r = \frac{\Delta V}{\Delta I} = \frac{1}{\text{slope}}$$

Fig. 71 V-I Characteristic curve for forward bias.

However, after a certain critical value of reverse voltage is reached, the silicon diode will show a rapid increase in reverse current. This voltage is called the *breakdown potential* of the diode. If the reverse current at this voltage is not limited, the diode will be destroyed. For many diodes, the breakdown voltage is about 50 V.

Reverse voltage breakdown (Avalanche breakdown)

The mechanism for production of enormous current at particular reverse bias voltage in the diode is *'avalanche' breakdown.* We have already seen that the electric field is intense in the depletion region near the junction. (Electric field = *p.d*/ distance)

The intense electric field accelerates the minority carriers in the depletion region. They make collisions with the valence electrons of outer orbits of atoms and make them free from the covalent bond. The newly liberated free electrons gain high energy to free again other valence electrons. The multiplication of free electrons and consequent increase of reverse current is known as *avalanche breakdown.*

Zener diode

A *p-n* junction diode, under reverse bias, shows a breakdown (current increasing rapidly) at a particular voltage. In a general purpose diode the doping is light. As a result, the breakdown voltage is high. If the diode is heavily doped, the breakdown voltage can be reduced. By doping the diode at different levels, the breakdown can be made to happen at any desired voltage V_z such as 5.1 V, 9.1 V etc. By making the *p-n* junction free from surface imperfections, a sharp breakdown can be obtained (fig. 74).

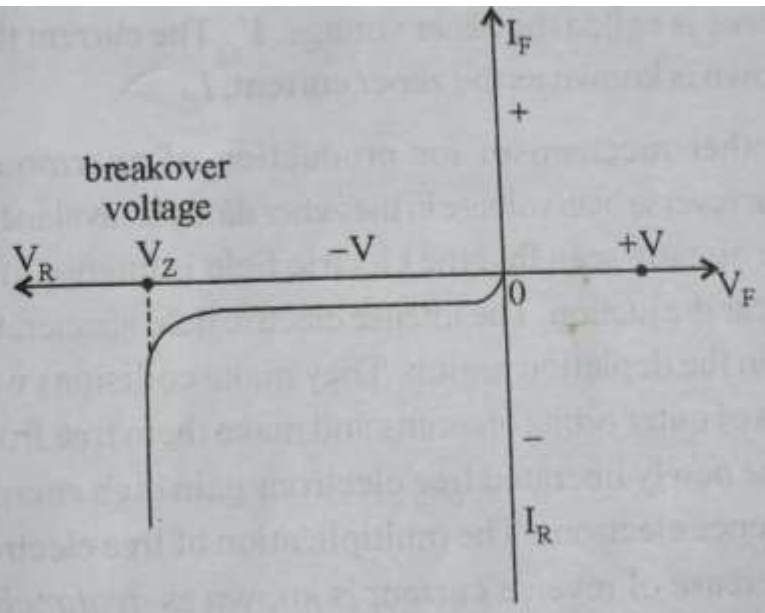


Fig. 74 Zener breakdown voltage

The diode, designed to work in the reverse breakdown condition continuously without being damaged but maintaining a constant voltage across its terminals is called Zener diode.

Zener diodes are used for voltage regulation purposes in electronic circuits. They are connected in the reverse bias condition and the voltage across the diode (V_z) remains constant, independent of the current passing through the diode.

Zener breakdown and avalanche breakdown: principle of Zener diode

When a junction is made up of heavily doped materials, the depletion region near the junction becomes very narrow. When a reverse bias is applied to the junction, a very intense electric field is set up across the depletion region. ($E = V/d$). The field is intense enough to pull the electrons from the valence orbits of atoms in the crystal. *i.e.*, the covalent bonds are broken. The creation of free electrons in this way and the consequent sudden surge of current at a particular voltage is known as the *Zener breakdown*. The reverse bias voltage at which the *Zener breakdown* takes place is called the zener voltage, V_z. The current that results after breakdown is known as the zener current, I_z.

Another mechanism for production of enormous current at a particular reverse bias voltage in the zener diode is 'avalanche' breakdown.

We have already seen that the electric field is intense in the deplection region near the juction. The intense electric field accelerates the minority carriers in the depletion region. They make collisions with the valence electrons of outer orbits of atoms and make them free from the covalent bond. The newly liberated free electrons gain high energy to free again other valence electrons. The multiplication of free electrons and consequent increase of reverse current is known as *avalanche breakdown.*

Zener breakdown is predominant for breakdown voltage below 6V.

The zener diode is not damaged during operation for reverse voltage and current lying within the power ratings given by the manufacturer. Power rating $P = V_z I_z$ watt, which is the electric power, that zener diode can withstand.

I-V characteristics of Zener diode

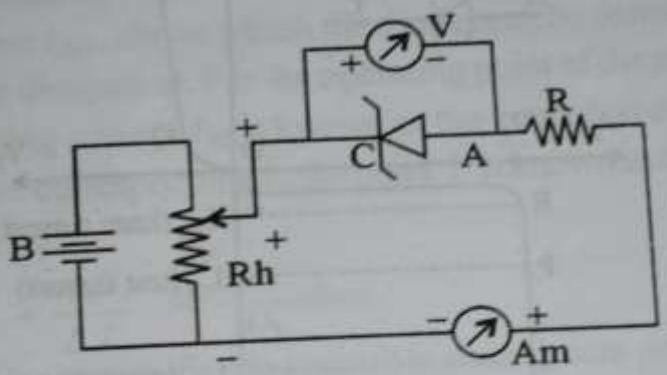


Fig. 75 Circuit diagram to draw I-V characteristics of zener diode.

Experiment The zener diode is connected for reverse bias as shown in figure 75. The current through the zener diode is measured with an ammeter A and the voltage across it using a voltmeter V. The potentiometer or rheostat is adjusted for $V = 0, -1, -2, -3, -4$, V etc and in each case the current I is measured. It is found that the current increases rapidly at a particular reverse voltage V_z. To control the sudden surge of current, a suitable limiting resistance R has to be used.

The experiment may be done connecting the zener diode for forward bias also. The variation of current I with the applied voltage V across the zener is shown in fig.

The forward characteristics is similar to ordinary silicon rectifier diode. It begins to conduct at 0.6 V. The reverse characteristics shows more or less constant current for voltage varying from zero upto the zener breakdown voltage V_z. Thereafter, the reverse current increases enormously. This may be due to zener breakdown or avalanche breakdown as explained earlier.

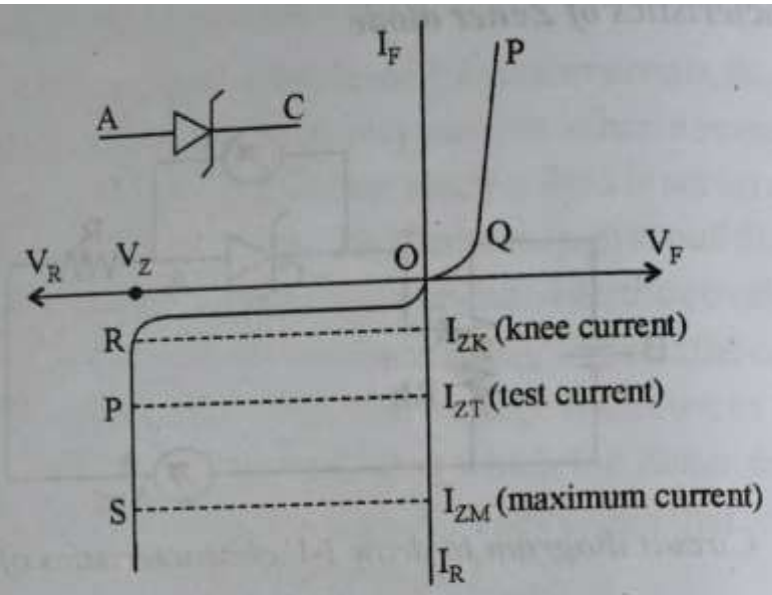


Fig. 76 I-V Characteristics of Zener diode.

Uses of zener diodes

1. The zener diodes can be used in voltage regulation circuits. A voltage regulator produces constant output voltage and it is independent of (*i*) the change of the load resistance and (*ii*) change of power supply voltage.

2. For fixing reference voltage in a network, for biasing and for calibrating voltmeters.

3. For clipping of voltage wave forms.

4. For meter protection against sudden increase of current throught the meter (Fig.). The voltage across the zener diode remains constant.

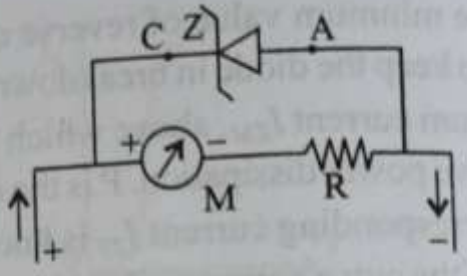


Fig. 78 Meter protection circuit using zener diode

The Tunnel Diode

Tunnel diode exhibits a phenomenon known as negative resistance. This means that an increase in forward voltage produces a decrease in forward current. It is a heavily doped *p-n* junction diode. Due to the heavy doping, the depletion layer is of very small thickness of the order of 10^{-5} m.

By definition, electric field $= \dfrac{\text{potential difference}}{\text{thickness of layer}}$

Even for a small forward or reverse bias, the electric field set up in the depletion region is extremely high. Hence the electrons having acquired sufficient energy due to the high electric field "tunnel" across the barrier and cross the junction even at low voltages (below 0.3 V). This happens both in forward and reverse bias conditions. Hence there is appreciable current even at low voltages.

The *V–I* characteristics of tunnel diode is shown in the figure. When the diode is forward biased, the current increases with increase of voltage up to 0.1 volt (point A). At A it begins to decrease with increase of voltage up to 0.3 volt. Beyond this, the current increases with voltage as in a normal *p-n* diode. This is shown by BC in the graph

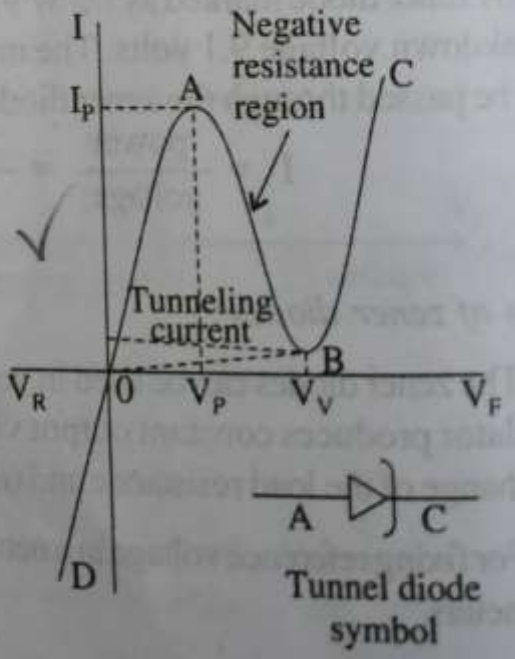


Fig. 79 Tunnel diode characteristics curve

When the diode is reverse-biased, due to the "tunnelling" effect the current increases with voltage. This is shown by DO.

We note that the current decreases with the increase of voltage in the region AB. This shows that the tunnel diode has a *negative resistance* behaviour in the region AB.

$$R_F = \frac{\Delta V_F}{\Delta I_F}$$

This result is opposite to that described in Ohm's law.

Principle of tunnel diode

In an ordinary diode, the depletion layer offers a barrier to the free flow of electrons from *n*-side to *p*-side. In a tunnel diode, due to heavy doping, the barrier width is considerably reduced and there are filled energy levels in theconduction band of the *n*-side. Corresponding to these energy levels, there are holes in the valence band of the *p*-side. As the width of the barrier is small, there is a finite probability that the electrons penetrate through the barrier and recombine with the holes having the same energy level in the valence band of the *p*-side. The probability for tunneling is found out using the principles of wave mechanics, where electron is treated as matter wave. The finite probability accounts for the current through the tunnel diode even with small voltage applied across the diode.

Figure shows the energy levels filled by electrons in the conduction band of *n*-side and the energy levels of the holes in the valence band of the *p*-side in a tunnel diode. The barrier width is narrow.

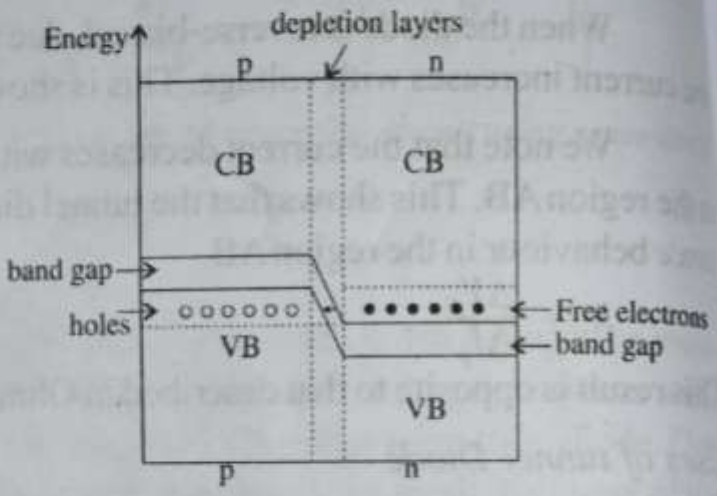


Fig. 80 Tunnel diode working principle : election tunneling from n→p

When a forward bias is applied, the energy levels on the *n*-side move up so as to reduce the barrier height. When there is mathcing of levels on the *n*-side and *p*-side, electrons tunnel through the depletion layer to the *p*-side and this causes the forward current. As the forward bias is further increased , the overlapping of the levels on either side is more and the current gradually increases and it becomes the maximum for maximum overlapping of energy levels. After this, the conduction band levels on the *n*-side rise above the valence band levels overlapping decreases and tunneling also decreases, resulting in the decrease of current for increase of voltage. This accounts for the negative resistance region of the *I-V* curve. The diode functions as ordinary diode for further increase of forward bias.

Uses of tunnel Diode

1. The tunnel diodes are used as high speed switches in computers. The high speed operation is made possible because of the fact that the tunnelling electrons move much more quickly than diffusing charge carrier. (holes and electrons).

2. The tunnel diodes are also used as high frequency amplifiers as they are much less sensitive to temperature changes than the transistors.

3. The tunnel diodes can be used as very high-frequency oscillators due to their negative resistance property.

Crystal diode as a rectifier

An electronic circuit that converts ac into pulsating dc is a rectifier. Rectifier is a part of a power supply.

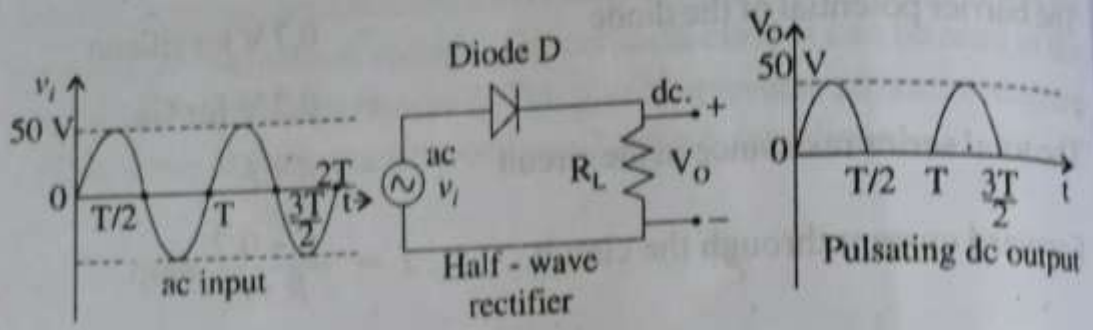


Fig. 73 Half - wave rectifier using one diode

Figure illustrates the rectifying action of a crystal diode. The a.c input voltage V_i to be rectified, the diode and load resistance R_L are connected in series. The output voltage V_o is obtained across the load resistance R_L. During the positive half cycle of input a.c voltage, the diode is forward biased and conducts current in the circuit.

The positive half-cycle of input voltage appears across R_L. During the negative half-cycle of input ac voltage, the diode is reverse biased. The diode does not conduct and no voltage appears across the load R_L. Here the output consists of positive half-cycles of input ac voltage while the negative half cycles are supressed. Thus the crystal diode changes a.c into d.c and works as a rectifier. The output voltage V_0 across R_L is pulsating d.c.

Half wave Rectifier

A p-n junction diode conducts current when it is forward biased. This property of the junction diode is used to covert an a.c. voltage into d.c. voltage. A circuit that converts an a.c. voltage into pulsating d.c. voltage is known as rectifier. Rectifier is one part of a power supply.

If the d.c output voltage is made available only during the time that input a.c. voltage is going through one half cycle. The rectifier is a half-wave rectifier.

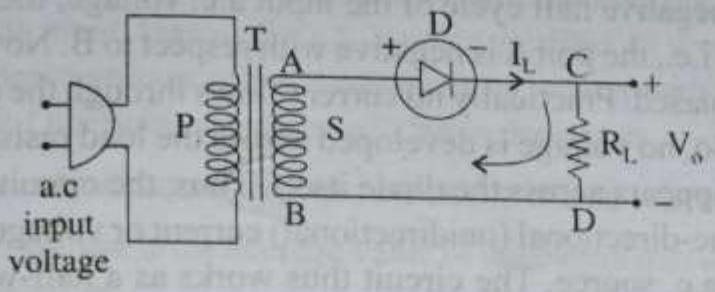


Fig. 81 Half wave rectifier using diode

Figure shows the circuit of a half wave rectifier. The primary of a transformer in connected to the power mains. An a.c. voltage is induced across the scondary of the transformer. The transfomer allows us to step up or step down the a.c. input voltage to the required level. Also the transformer isolates the rectifier circuit from the power line. The induced voltage (v) can be represented by the equation.

$$v = V_m \sin \omega t$$

where V_m is the peak voltage and ω is the angular frequency of the alternating current. During positive half cycle of the input a.c. voltage, the upper end A of the transformer secondary goes through a positive half sine wave. This means, the diode is forward biased. During the negative half cycle of the input, the secondary winding has negative sine wave at A. During this time, the diode is reverse biased. Thus, for every input a.c. cycle, the diode is forward biased for half the cycle.

During the time that the diode is forward biased, it conducts current in the forward direction of the diode (p to n). Let the current be i_L and it flows through the load R_L and the entire series circuit. This current makes the upper end C at the output side positive with respect to the terminal B. Since a forward biased diode offers a very low resistance, the voltage drop across it is also very small (about 0.3 V for

During negative half cycle of the input a.c. voltage, the polarity ge reversed i.e., the poit A is negative with respect to B. Now the diode i reverse biased. Practically no current flows through the diode and th circuit. So, no voltage is developed across the load resistance. All th voltage appears across the diode itself. Thus, the circuit arrangemen makes one-directional (unidirectional) current or voltage at the outpu from an a.c. source. The circuit thus works as a half-wave rectifier Since the output does not change polarity, it is a pulsating d.c. voltage with a frequency equal to that of the input frequency.

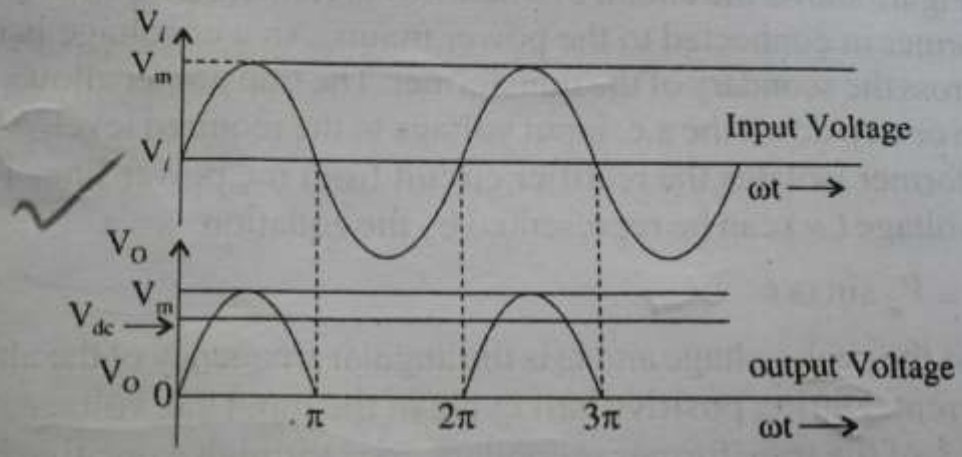


Fig. 82 Half wave rectifier :
input and output voltage wave forms

The input and output waveforms are shown in the figure. T output voltage V_0 across the load, though not a perfect d.c., is a unidi tional voltage.

Full-wave Rectifier

Full wave rectifier is the most commonly used rectifier type in the dc power supplies. Full wave rectifier allows (one-way) current through the load during the entire 360^0 of the input cycle. The output is a pulsating d.c. current with a frequency twice the input frequency that pulsates every half-cycle of the input.

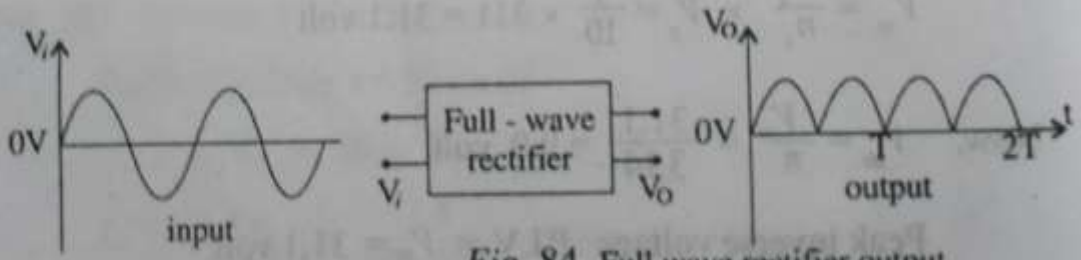


Fig. 84 Full wave rectifier output

The following two circuits are commonly used for full-wave rectification:
(i) Centre tap full- wave rectifier and (ii) Full - wave bridge rectifier.

Centre - Tap Full-wave rectifier

A full-wave rectifier converts a.c. into d.c. and provides d.c. output through the load in the same direction for both half cycle of the a.c input. Since the diodes conduct only in one direction, two diodes are connected to the secondary of a centre-tapped transformer.

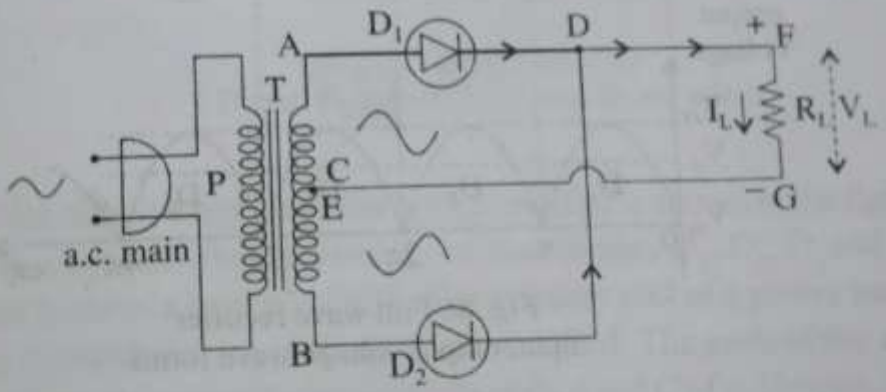


Fig. 85 Full wave rectifier

The rectifier circuit of consists of a step-down centre-tap transformer (T) with the secondary end points A and B and the centre tap, C. The primary (P) of the transformer is connected to a.c. mains. The ends of the secondary are connected to the anodes of the diodes D_1 and D_2, as shown in the figure. R_L is the load resistance, across which rectified d.c. will be available. C is the common point (floating ground) of the rectifier circuit. a.c. voltage is measured with respect to the point, C.

When the a.c. mains is switched on, a stepped down a.c. voltage is available at the secondary of the transformer. At one instant, when the point A is positive, the point B will be negative with respect to the common point C and vice-versa.

In one half cycle of a.c., when the point A is positive, the diode D_1 is forward-biased and D_2 is reverse-biased. This makes D_1 to conduct current through the load from F to G.

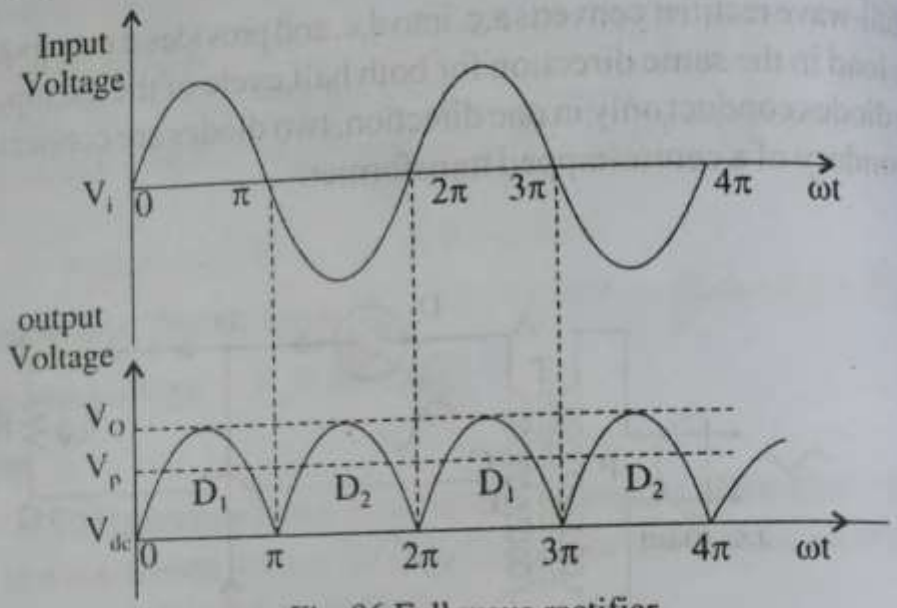


Fig. 86 Full wave rectifier
input, output voltage wave forms

In the next half cycle, the point B is positive with respect to C. The diode D_2 is now forward biased and D_2 now conducts current to flow through the load resistance from F to G. Thus, in both half cycles, the direction of the current is from F to G in the load resistance. The whole process repeats for each cycle of a.c. input. Thus, the circuit acts as a full-wave rectifier, converting a.c. into d.c.

The full-wave rectifier inverts each negative half cycle, so that we get double the number of positive half cycles. The frequency of the full-wave signal is double the input frequency. ie, $f_{out} = 2f_{in}$

Full-wave Bridge rectifier

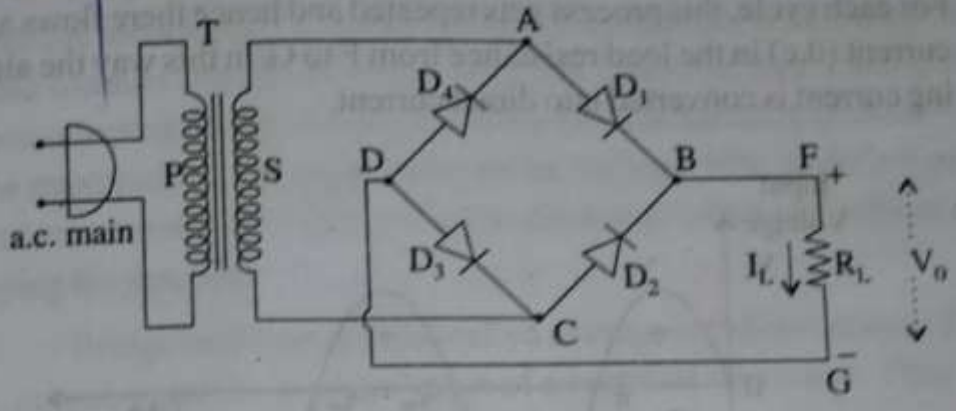


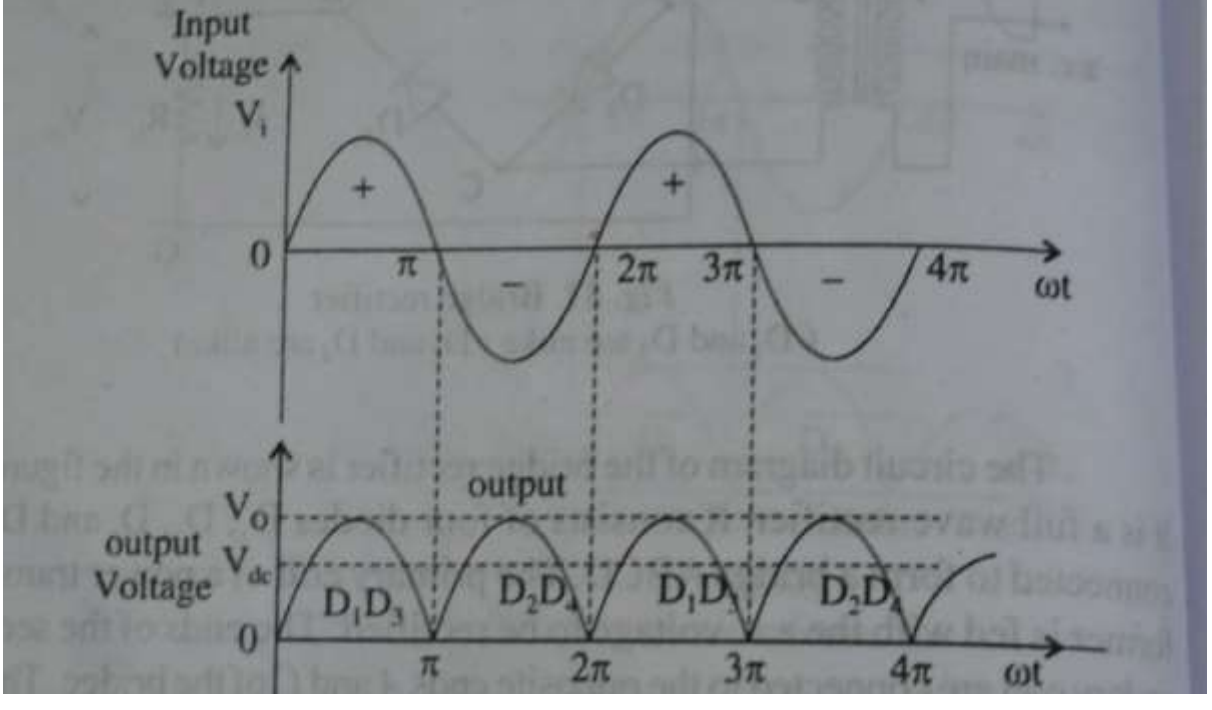
Fig. 87 Bridge rectifier
(D_1 and D_3 are alike ; D_2 and D_4 are alike)

The circuit diagram of the bridge rectifier is shown in the figure It is a full wave rectifier. It consists of four diodes D_1, D_2, D_3 and D_4 connected to form a bridge ABCD. The primary coil of a power transformer is fed with the a.c. voltage to be rectified. The ends of the secondary coil are connected to the opposite ends *A* and *C* of the bridge. The other two ends B and D are connected to resistance R_L (load).

Working

The a.c. main voltage applied to the primary of the transformer induces e.m.f in the secondary coil. the voltage is stepped down. During the positive half of the cycle of the induced e.m.f, let the end A be positive and C be negative. Now, the diodes D_1 and D_3 are forward biased; and D_2 and D_4 are reverse biased. Hence the diodes D_1 and D_3 conduct current. As these two are in series with the load resistance R_L and the transformer secondary, a current flows through the load in the F to G direction. This makes the end F positive with respect to G.

During the negative half cycle of a.c. the end C becomes positive with respect to A. This makes the diodes D_2 and D_4 forward biased, whereas the diodes D_1 and D_3 are reverse-biased. Hence the diodes D_2 and D_4 conduct, causing the current flow again from F to G in the load resistance. Thus, the end F is again positive with respect to the point G. For each cycle, this process gets repeated and hence there flows a direct current (d.c) in the load resistance from F to G. In this way the alternating current is converted into direct current.



Advantages

1. In a bridge rectifier, the transformer secondary is fully used for each half cycle and there is no need for centre-tap. As the need for a centre-tap transformer is eliminated, the transformer cost is reduced.

2. The output of a bridge rectifier is twice that of a centre-tap rectifier for the same secondary voltage of the transformer.

3. The peak inverse voltage is half of that of the centre-tap rectifier.

Disadvantages

1. Four diodes are required instead of two diodes. This increases the cost of the rectifier.

2. During each half cycle of the a.c. input, two diodes will be conducting in series. Therefore the voltage drop across the forward resistance of the rectifier diodes will be twice that in the centre-tapped rectifier. This becomes a serious problem when the secondary voltage is small.

Comparision of rectifiers

1. The output of the half wave rectifier $\left(\frac{I_m}{\pi}\right)$ is low compared to the output of full-wave rectifier $\left(\frac{2I_m}{\pi}\right)$

2. The efficiency of full-wave rectifier (81.1 %) is twice that of Half-wave rectifier (40.6%).

3. The peak inverse voltage of half-wave rectifier is V_m. PIV of centre tap rectifier is $2V_m$ and PIV of Bridge rectifier is V_m.

4. The output pulsating frequency of half-wave rectifier is same as input ac frequency $f_{out} = f_{in}$

5. Current flows through the transformer secondary in one direction only in the half-wave rectifier. This saturates the core of the transformer, which increases the hysteresis loss and produces the harmonics in the secondary output.

Filter Circuits

The output of a full wave rectifier is uni-directional but it is pulsating (not steady). The output voltage consists of a pure d.c. voltage along with an a.c. component (pulsating), called ripple. The ripples must be removed or reduced from the rectifier output, so as to get constant d.c. output voltage. This is done by introducing an electrical network between the rectifier and the load. Such as a net work is known as filter, smoothing circuit.

A filter circuit is a device which removes the a.c. component of the rectifier output that allows the d.c. component to reach the load.

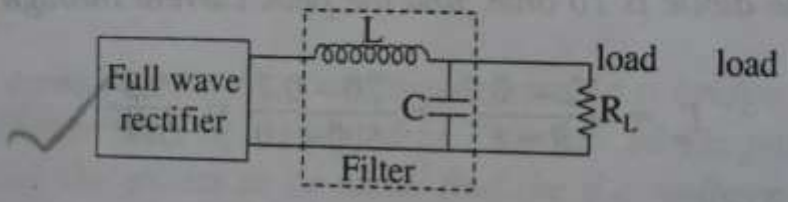


Fig. 92 L.C. *choke - input* filter

A filter can be constructed using a combination of inductance (L) and capacitor (C). A capacitor passes a.c. but does not allow d.c. An inductance passes d.c. but it opposes a.c. Thus a suitable combination of L and C is useful to form a filter that can remove a.c. component in a rectifier output, while allowing the d.c. component to reach the load.

The capacitor-input filter (Shunt Capacitor Filter)

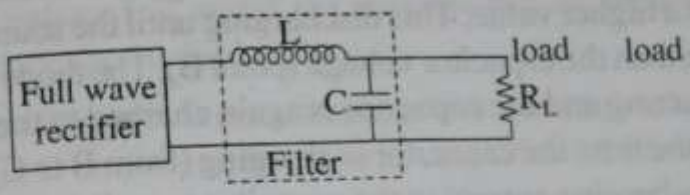


Fig. 92 L.C. *choke - input* filter

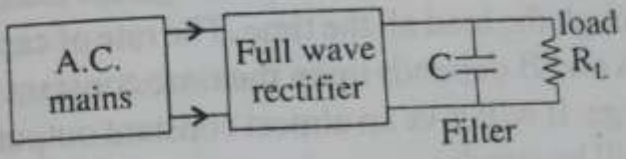


Fig. 93 *Capacitor input* filter

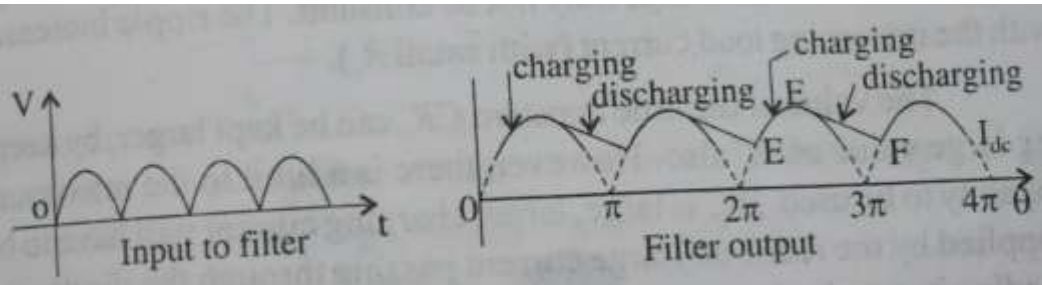


Fig. 94 Rectified and filtered output voltage wave form of full wave rectifier with capacitor input filter

The arrangement shows a simplest and cheapest filter. The rectifier feeds directly into the capacitor and so the filter is called capacitor-input filter. The capacitor is connected across the rectifier output. The capacitor is shunted with the load resistor, R_L.

When the rectifier output is increasing (shown by OA). the capacitor charges to peak voltage V_m. Just after this, the rectifier output begins to fall (shown by the dotted curve). At this time, the source voltage becomes slightly less than V_m. This puts the diode in the rectifier

under reverse bias. The diode stops conducting. The capacitor discharges through R_L and it delivers its stored energy to R_L and maintains the voltage across R_L at a higher value. This discharging until the source voltage becomes more than the capacitor voltage (point B). The diode in the rectifier starts conducting and the capacitor is again charged to the peak voltage V_m. During the time the capacitor is charging (from B to C), the rectifier supplies the charging current to the capacitor as well as load current i_L.

When the capacitor discharges, the rectifier does not supply any current but the capacitor sends current i_L through the load. The current is maintained through the load all the time. The rate of capacity or discharge between A and B depends upon the time constant (CR_L). If the value of CR_L is large, It will give an almost constant output voltage and the load current will be steady.

If R_L is large, the discharge is slow. If R_L is small, the discharge is rapid and the load voltage may not be constant. The ripple increases with the increasing load current (with small R_L).

The value of the time constant CR_L can be kept larger, by keeping large value of C also. However, there is a limit to the maximum capacity to be used. If C is large, larger charging current will have to be supplied by the rectifier. Large current passing through the diode, exceeding its rated value, may damage the diode.

If f is the frequency of the a.c mains supply (input), the frequency of the rectified output in the full wave rectifier is $(2f)$.

The period $T = \frac{1}{(2f)}$

The choke - input LC filter

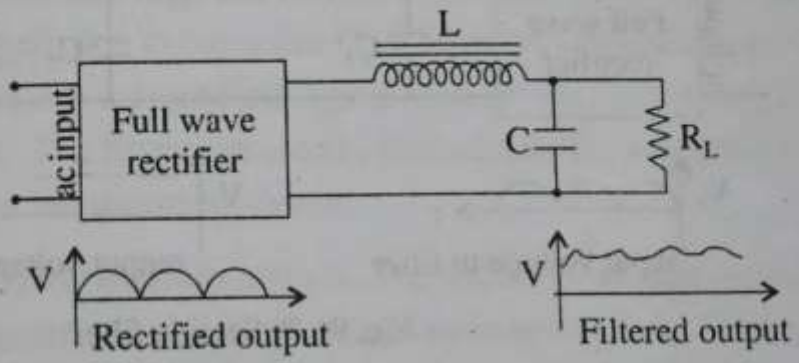


Fig. 95 Full wave rectifier with an L.C. Choke input filter

Figure shows a full wave rectifier having a choke L (iron-core inductor), a capacitor C and load resistor R_L. The output from the full wave rectifier consists of a *d.c.* component (which we want to pass through R_L) and an a.c. component (unwanted).

Working

The choke allows the d.c. component to pass through easily since the reactance $X_L = L\omega = 0$ for $\omega = 0$ with *d.c.* But for $\omega = 0$, the reactance of capacitor is $X_C = 1/C\omega = 1/0 = \infty$ for d.c. So the capacitor is open for d.c. current. Hence all the d.c. current out of the choke passes through the load resistance R_L.

Considering the a.c component, the choke blocks the a.c. component because the reactance $X_L = L\omega$ = high at high frequency like 100 Hz. More over, any a.c. current that happens to pass through the choke also passes through the capacitor rather than the load R_L the capacitative reactance $X_C = (1/C\omega)$ is smaller than R_L. In other words, the choke and the capacitor act as an a.c. voltage divider and brings out only very small atenuated a.c. component in the final output. Thus the filter enables us to get a constant voltage across the load resistor R_L.

The π-filter

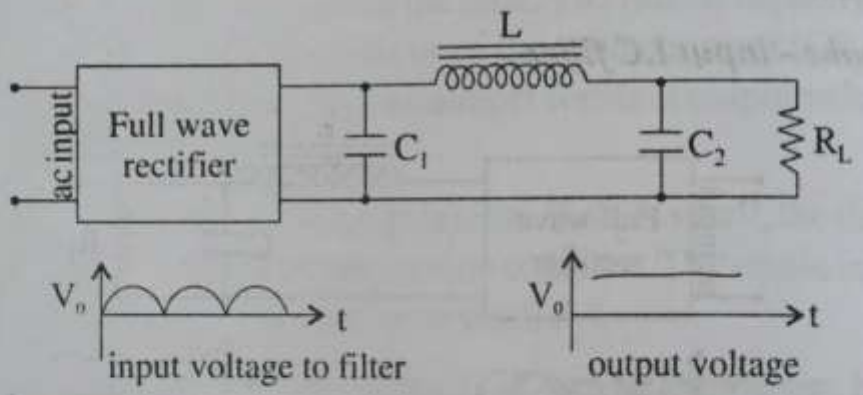


Fig. 96 Pi Section filter

The π-filter consists of two capacitors C_1 and C_2 and an inductor L, connected in the shape of the Greek letter π as shown in the diagram.

Working

The pulsating output from the rectifier is applied across the input terminals AB of the filter. A constant output voltage, free from ripples, is made available across the load resistor R_L. The functions of various components in the filter are described below :

(i) The filter capacitor C_1 offers low resistance to a.c. component in the rectified output. But it offers infinite risistance to d.c. component. Therfore,

the capacitor C_1 by-passes a.c. component whereas the d.c. component reaches the choke L.

(ii) The choke L offers high resistance to the a.c. component. But it offers almost zero resistance to the d.c. component and it allows the d.c component to flow through it, while the a.c. component is blocked.

(iii) The capacitor C_2 by-pass the a.c. component which could not be blocked by the choke. Therefore, only d.c. component appears across the load and we get a constant output voltage, free from ripples For improving smoothing action, several identical π sections are used.

The π filter generates high out voltage at low current drains. It provides high voltage gain due to capacitor C_2. The output voltage drops rapidly with the increase in current flowing the load. So the voltage regulation of π filter is poor. The filters are used to demodulate the particular range of frequency in communication device.

The π filter has some disadvantages. The inductors are heavy and costly. Moreover, the series inductor produces an external field. Hence the series inductor is replaced by a high wattage low resistance.

Zener diode as voltage regulator

A voltage regulator is an electronic circuit that produces a *constant output voltage* V_0 even if there is variation of input supply voltage V_s or if there is any variation of load current I_L due to change of load R_L.

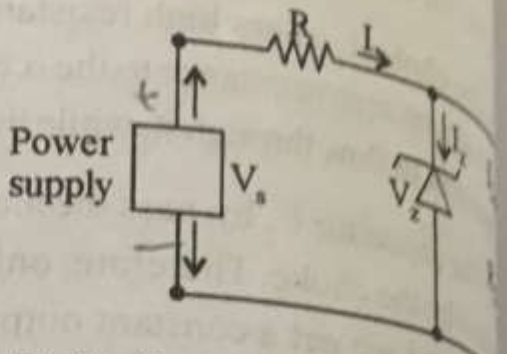


Fig. 97 Zener diode as voltage regu

Figure 72 shows a voltage regulator circuit. V_s is the output voltage from a power supply. R_L is the load across which we wish to have constant output voltage. achieved with the use of a zener diode and a current limiting resi The zener diode is connected in its reverse bias mode.

Let I be the current through R and V_z be the zener voltage. If the supply voltage, by Kirchoff's voltage law,

$$V_s = IR + V_z$$

Case (i) Due to any change in the supply voltage, there will corresponding change in the current I. When V_s increases, the voltage drop across R also increases, since V_z = constant. When V_s decreases the value of the voltage drop ($I R$) decreases proportionately as V_z = constant. Thus, change of supply voltage does not affect the output voltage V_o which is voltage across the load.

Case(ii) Now consider that the supply voltage V_s is constant, supplying constant current I, but the load R_L is changing. The main current divides into two branch currents (i) through the zener diode as I_z and through the load as I_L. By current summation,

$$I = I_z + I_L$$

Let the load current I_L decrease due to change of load. Since the main current is constant in the circuit, the value of I_z correspondingly increases. Yet the voltage across the zener diode V_z remains constant. This makes the output V_0 constant irrespective of the change in the load. On the other hand, when the load current I_L is increased, the zener current decreases but V_z still remains constant. giving out constant output voltage, V_0.

Thus the circuit (fig.) functions as a voltage regulator. The voltage regulation factor (VRF) is defined as the ratio

$$\text{VRF} = \frac{(V_o)_{\text{no load}} - (V_o)_{\text{full load}}}{(V_o)_{\text{full load}}}$$

If the VRF is smaller, the voltage regulation will be better.

QUESTIONS FROM BOOKS

Questions

1. What is a p-n diode? Describe potantial barrier and 'depletion region' in p-n junction diode.

2. Describe with suitable graphs, the action of p-n diode under (i) forward bias and (ii) reverse bias.

3. Sketch the forward and reverse characteristics of p-n junction diode and define knee voltage, reverse break down voltage and reverse saturation current and diode dynamic resistance.

4. Describe the method of obtaining the diode characteristics. Sketch the forward and reverse characteristics of the diode.

5. Explain rectifying action of p-n junction diode.

6. What is a zener diode? Sketch its forward and reverse characteristics. Define zener breakdown voltage.

7. Describe an experiment to draw I-V characteristics of a zener diode. List out the uses of zener diode.

8. Explain the principle of zener breakdown. Distinguish between 'zener breakdown' and 'Avalanche breakdown'.

9. Explain the action of zener diode as voltage regulator.

10. Show that the voltage across the zener diode in a voltage regulator is independent of zener current variations and load resistance.

11. Describe the working of a half-wave rectifier using crystal diode. Derive expressions for (i) output d.c. voltage and (ii) efficiency of half-wave rectifier. What are the disadvantages of half-wave rectifier?

12. Give the block diagram of a regulated power supply and explain the function of various units in it.

13. Describe the working of a full-wave rectifier using crystal diodes and derive the expressions for (i) average current, (ii) r.m.s current, (iii) ripple factor and rectifier efficiency.

14. Giving circuit diagram, explain the working of a bridge rectifier. What are its advantages and disadvantages?

15. What is a tunnel diode ? Describe its construction and uses. Explain the principle of working of a tunnel diode, giving its I – V characteries.

16. What is the function of a filter in a power supply? Explain the action of π filter.

17. Describe the action of the following filter circuits :

(i) Capacitor filter (ii) Choke input filter and

(iii) Capacitor input filter.

18. Define ripple factor, peak inverse voltage and efficiency of a rectifier. Deduce the value of ripple factor of half-wave rectifier.

Objective type questions

1. The depletion region in a p-n junction diode is formed due to

(a) doping (b) barrier potential (c) bound ions (d) biasing

2. What is the built-in-potential of a silicon diode at room temperature?

(a) 0.7 V (b) 0.3 V (c) 1 V (d) 2 mV/°C

3. The voltage at which avalanche occurs in a diode is called

(a) barrier potential (b) depletion layer

(c) knee voltage (d) breakdown voltage

4. When the reverse voltage increases from 5 to 10 V in a diode, the depletion layer width becomes

(a) smaller (b) larger (c) unaffected (d) breakdown

5. The knee voltage of a diode is approximately equal to

(a) applied voltage (b) barrier potential

(b) breakdown voltage (c) forward voltage

6. A diode in a circuit is in series with 220 ohm resistor. the p.d across the resistor is 4 volt. The current through the diode is

(a) 50 A (b) 0.7 A (c) 0.02 A (d) 0.2 A

7. A diode has a voltage of 0.7 V across it. When a current of 50 mA is passed through it, the power dissipated by the diode is

(a) 35 mW (b) 71.4 mW (c) 0.014 W (d) 0 W

8. Silicon diodes are preferable in rectifiers to germanium diodes because of its

(a) large reverse saturation current (b) small reverse saturation current

(c) low cost (d) high breakdown voltage

9. Reverse bias current in a diode is of the order of

(a) kA (b) mA (c) μA (d) A

10. Crystal diode is used as

(a) amplifier (b) rectifier

(c) oscillator (d) voltage regulator

11. A zener diode is always _____ connected.

(a) reverse bias (b) forward bias

(c) either reverse or forward bias (d) none of the above.

12. In the breakdown region, a zener diode behaves like a _____ source.

(a) constant voltage (b) constant current

(c) constant resistance (d) none of the above

13. The average value of a half wave rectified voltage with a peak value of 200 V is

(a) 63.7 V (b) 127.3 V (c)141 V (d) 0 V

14. When a 50 Hz sinusoidal voltage is applied to the input of a half-wave, the output frequency is

(a) 100 Hz (b) 25 Hz (c) 50 Hz (d) 0 Hz

15. The peak value of the input to half-wave rectifier is 10 V. The peak value of the output is

(a) 10 V (b) 3.18 V (c) 10.7 V (d) 9.3 V

16. The average value of a full-wave rectified voltage with a peak value of 75 V is

(a) 53 V (b) 47.8 V (c) 37.5 V (d) 23.9 V

17. When a 50 Hz sinusoidal voltage is applied to the input of a full-wave rectifier, the output frequency is

(a) 100 Hz (b) 50 Hz (c) 200 Hz (d) 0 Hz

18. Which of these is the best description of a zener diode ?

(a) it is a rectifier diode

(b) It is a constant - voltage device

(c) It is a constant - current device

(d) It works in the forward region

19. If one of the diodes in a bridge full-wave rectifier opens, the output is

(a) 0 V

(b) one - fourth the amplitude of the input voltage

(c) a half-wave rectified voltage (d) a 120 Hz voltage

20. If you are checking a 50 Hz full-wave bridge rectifier and observe that output has a 50 Hz *ripple*,

(a) The circuit is working properly

(b) There is an open diode

(c) The transformer secondary is shorted

(d) The filter capacitor is leaky.

21. A 10 V peak-to- peak sinusoidal voltage is applied across a silicon diode and series resistor. The maximum voltage across the resistor is

(a) 9.3 V (b) 5 V (c) 0.7 V (d) 10 V (e) 4.3 V

22. A device that exhibits negative resistance behaviour is

(a) crystal diode (b) Zener diode (c) tunnel diode

(d) all the above

23. Ripple factor is

(a) $\frac{I_{rms}}{I_{d.c}}$ (b) $\frac{I^2_{rms}}{I^2_{d.c}}$ (c) $\sqrt{\frac{I_{rms}}{I_{dc}} - 1}$ (d) $\sqrt{\frac{I^2_{rms}}{I^2_{dc}} - 1}$

Answers

1. (c)	2. (a)	3. (d)	4. (b)	5. (b)	6. (c)
7. (a)	8. (b)	9. (c)	10. (b)	11. (a)	12. (a)
13. (a)	14. (c)	15. (d)	16. (b)	17. (a)	18. (b)
19. (c)	20. (d)	21. (d)	22. (c)	23. (d)	

UNIT-III

TRANSISTOR AMPLIFIERS

Transistor action - Transistor connections - common emitter - common base -common collector - analysis of amplifiers using h- parameters - RC coupled amplifier - transformer coupled amplifier - power amplifier - classification of power amplifiers (Class A, Class B and Class C)- Push pull amplifier - FET charecteristics - JFET characteristics

Junction transistor (Bipolar Junction Transistor - BJT)

A transistor consists of a semi-conductor material such as silicon or germanium. The material is doped to from three regions *p*, *n* and *p* with two junctions J_1 and J_2 so as to get a *p-n-p* transistor. The BJT is a bipolar device involving both types of charge carriers - electron and holes.

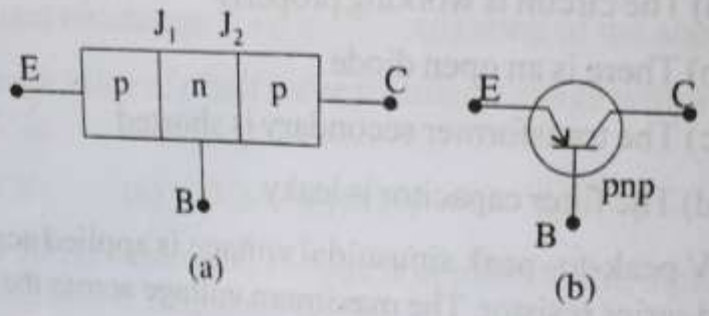


Fig. 106

The middle region is relatively thin and lightly doped. Connecting leads are provided in the three regions to make electrical connections. The lead E is called the 'emitter'. There are two juncitions J_1 and J_2 in the transistor. The junction J_1 is known as the emitter-base junction and the junction J_2 is known as the collector-base junction. Each junction acts as a *p-n* diode. The circuit symbol of the *p-n-p* transistor is shown in fig.

A *n-p-n* transistor can be formed in a similar way by forming a *n*-region, *p*-region and *n*-region. The base region is lightly doped. The leads E, B and C represent the emitter, base and collector regions respectively. The circuit symbol is shown in fig. This can be distinguishable from the *p-n-p* transistor by the arrow mark on the emitter side. The arrow mark is always from *p* to *n* to indicate the direction of the current.

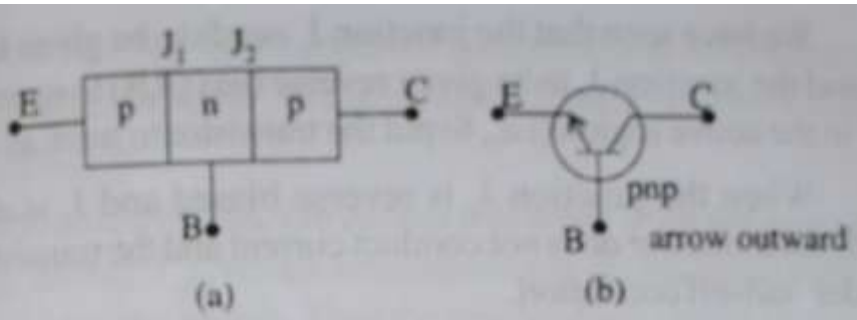


Fig. 107

Biasing the transistor for active region

Biasing means applying d.c. voltages across the junctions for the working of the transistor. The emitter-base junction J_1, is forward-biased and the collector-base junction J_2 is reverse-biased. The biasing connections are shown below.

It is known that electrons are the majority current carriers in *n*-region and 'holes' are the minority carriers here. Similarly 'holes' are the majority current carries in the *p*-region and electrons are the minority carriers there.

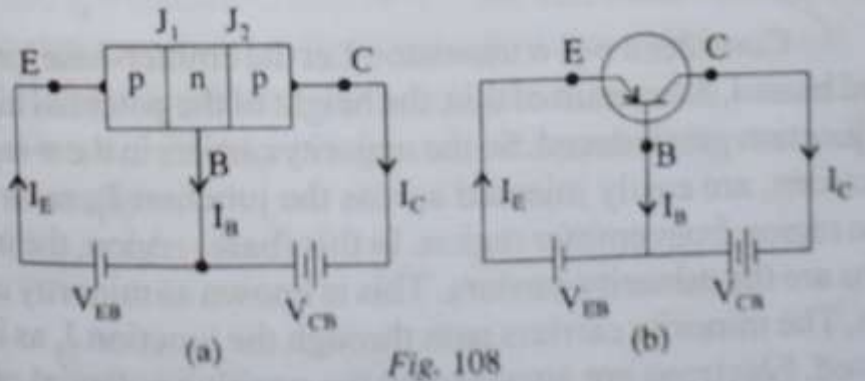


Fig. 108

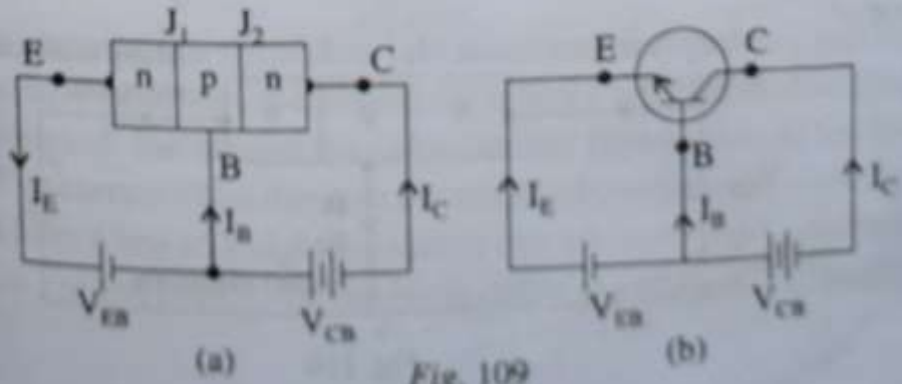


Fig. 109

We have seen that the junction J_1 needs to be given forward bias (FB) and the junction J_2 to be given reverse bias (RB) to operate the transistor in the active region (i.e., to put the transistor to work as amplifier).

When the junction J_1 is reverse biased and J_2 is also reverse biased, the transistor does not conduct current and the transistor is said to be under 'cut-off condidion.

When J_1 and J_2 are both forward biased, the transistor conducts maximum courrent through it (depending upon the bias voltages and circuit components) and it is said to be in 'saturation'. We summarise the above results as follows.

J_1	J_2	Transistor condition
FB	RB	active
RB	RB	cut - off
FB	FB	saturation

Transistor action

Consider a *n-p-n* transistor. Let the emitter-base junction be forward biased. As a result of this, the height of the potential hill (barrier) at the junction gets reduced. So the majority carriers in the *n*-region, namely electrons, are easily injected across the junction J_1, so as to reach the base region from emitter region. In this (base) region, the injected electrons are the minority carriers. This is known as minority carrier injection. The minority carriers pass through the junction J_2 as it is reversed biased. Electrons are attracted by the positive potential of the battery V_{CB}.

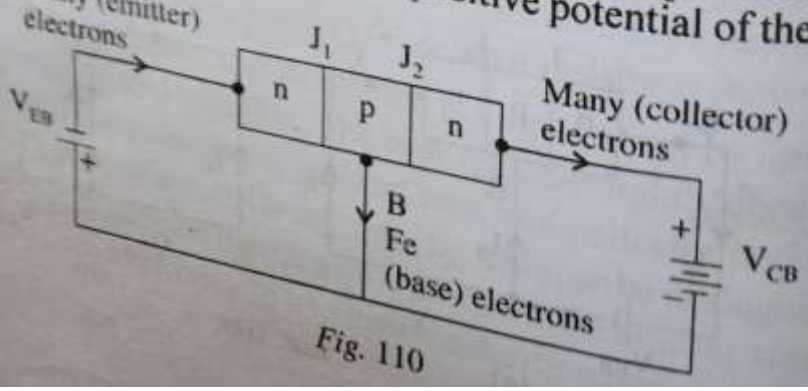


Fig. 110

However, a few of the injected electrons will be lost due to recombination with the 'hole' in the *p*-region (base) i.e., there is loss of holes in the *p*-region.

To balance this loss, the excess electrons from the base are received by the battery V_{EB}, which simultaneously drives equal number of electrons to the emitter region. Thus the emitter-base circuit is complete. The flow of electrons in the completed circuit constitutes the base current I_B.

The electrons crossing the junction J_2 reach the collector regions where they are the majority carriers. These electrons are pulled towards the battery V_{CB}, which drives equal number of electrons to the emitier region. The circuit is completed around the transistor. The flow of electrons in the completed circuit forms the collector current I_C. The emitter current (I_E) is the sum of the base current and the collector current. i.e.,

$$I_E = I_B + I_C$$

For example, in an ordinary transistor, for $I_E = 1$ milliampere (mA) $I_C = 0.98$ mA and $I_B = 0.02$ mA, i.e., 98% of the electrons injected by the emitter into the base reach the collector and flow through the circuit. The ratio (I_C / I_E) is called *transistor alpha*, α (d.c. alpha) or common base current gain. The ratio (I_C / I_B) is konwn as transistor β (d.c.beta) common emitter current gain.

$$\alpha = \frac{I_C}{I_E}$$

$$\beta = \frac{I_C}{I_B}$$

The emitter-base circuit has low resistance for current since it is forward biased. The collector-base circuit offers a high resistance since it is reverse biased. But almost the same current flows through the two junctions. The current-flow through the emitter base junction J_1 is thus transferred from a low to a high resistance circuit, as if there is transfer of resistance. For this reason, the device is called the transistor (transfer-resistor).

Relation connecting α and β of a transistor

Let a *n-p-n* transistor be biased to work in the active region. The emitter, base and collector current directions are shown in the figure

By definition, transistor $\beta = I_C / I_B$)

and $\alpha = I_C / I_E$)

From transistor action, $I_E = I_B + I_C$

$\therefore \quad I_C = (I_E - I_B)$

Using this in $\alpha = (I_C / I_E)$,

$$\alpha = \frac{I_E - I_B}{I_E}$$

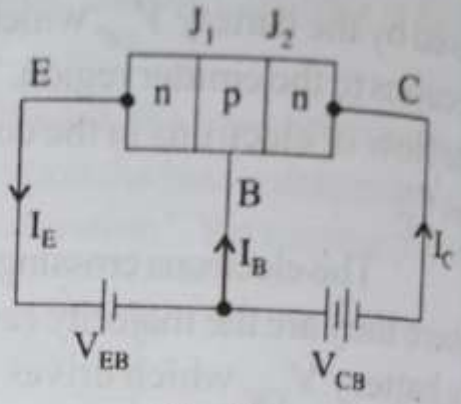


Fig. 111

Dividing each term in the r.h.s. by I_C

$$\alpha = \frac{(I_E / I_C) - (I_B / I_C)}{(I_E / I_C)}$$

$$\alpha = \frac{(1/\alpha) - (1/\beta)}{(1/\alpha)}$$

$$\therefore \alpha\left(\frac{1}{\alpha}\right) = \left(\frac{1}{\alpha}\right) - \left(\frac{1}{\beta}\right)$$

$$\therefore \left(\frac{1}{\alpha}\right) - \left(\frac{1}{\beta}\right) = 1.$$ From this, we get other relations as

$$\beta = \frac{\alpha}{1-\alpha} \text{ and } \alpha = \frac{\beta}{1+\beta}$$

The three modes of transistor connection

A transistor is first of all to be biased properly for using it as amplifier. When an input signal (v_i) is applied, the transistor circuit produces a desired output signal (v_0) across a load.

A transistor may be connected in three different modes. The first one is with the base kept common to the input signal voltage and the

output signal voltage. This mode of connection is known as the common base (CB) mode (fig.). The output v_0 is taken across the load resistance R_C.

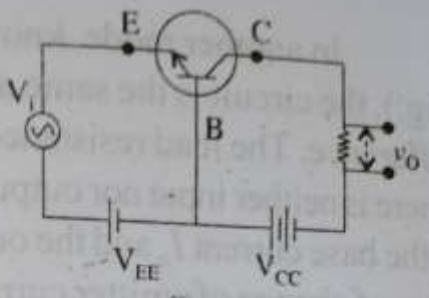


Fig. 112

Let input signal voltage = v_i. Output signal voltage = v_0 Then, voltage gain $A = v_0 / v_i$

If ΔI_C is the variation of collector current for the variation of emitter current ΔI_E at constant collector potential, then a.c. *alpha* of a transistor is defined as

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

Similarly, in *common emitter* (CE) mode (fig.), the input voltage v_i is applied between the base and the emitter and the output voltage is available between the collector and the emitter.

If ΔI_c is the collector current variation for the base current variation $\Delta 1_B$ keeping the collector voltage constant, the ratio $(\Delta I_C / \Delta I_B)$ is called the a.c. transistor beta (h_{fe})

$$\text{a.c. transistor } \beta = h_{fe} = \frac{\Delta I_C}{\Delta I_B}$$

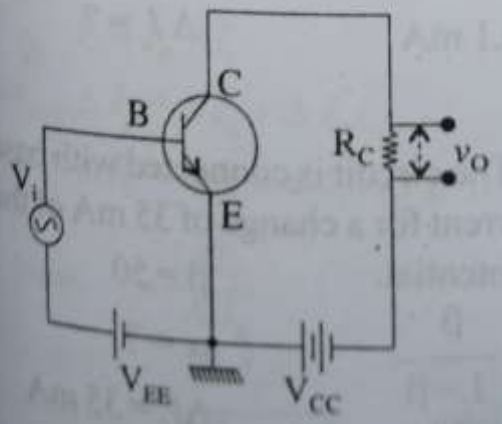


Fig. 113

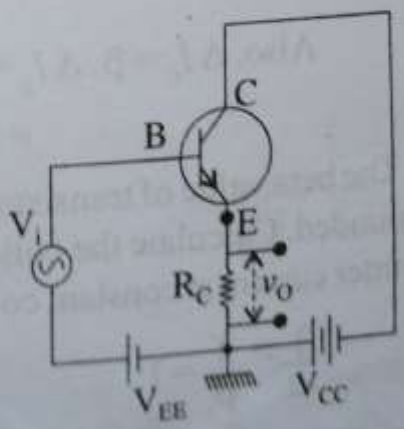


Fig. 114

In another mode, known as the common collector (CC) mode (fig.), the circuit is the same as the common emitter circuit, but with a difference. The load resistance is in the emitter circuit in the CC mode. There is neither input nor output in the collector circuit. The input current is the base current I_B and the output current is the emitter current I_E. The ratio of change of emitter current ΔI_E to the change in base current ΔI_B is known as current amplification factor γ of the CC circuit.

$$\gamma = \frac{\Delta I_E}{\Delta I_B}$$

Comparison of transistor connections

Characteristics	CE	CB	CC
1. Input impedance	low (750Ω)	low (100Ω)	very high (759 kΩ)
2. Output impedance	high (45k Ω)	very high (450 kΩ)	low (50Ω)
3. Voltage gain (A)	About 500	About 150	about 1
4. Application	For audio amplifier	Used in high frequency circuits	For impedance matching.

Analysis of a transistor CE amplifier using h-parameters

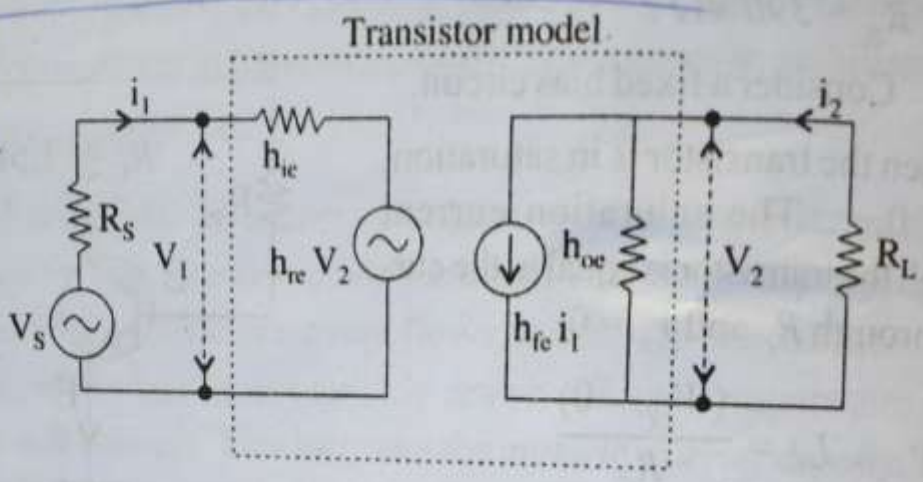


Fig. 117

Figure shows the h-parameters equivalent circuit of a common emitter transistor amplifier. The dotted box represents h-parameter model of the transistor, where

h_{ie} is the input impedence; (the subscript e is added to represent the common emitter mode)

h_{oe} is the output admittance;

h_{fe} is the forward current gain;

h_{re} is the reverse voltage transfer ratio of the transistor.

The signal source V_S is across the input port along with its source impedence R_S. The load resistance R_L appears across the output port. v_1 and v_2 are the input and output signals respectively. The input and output currents are taken to be positive, while flowing inward. The circuit is an a.c. equivalent circuit and d.c. values do not appear in the circuit.

Let i_1 and i_2 be the input and output currents, with the presence of the source and load. The equations for the input voltage and output current are (The independent quantities are "I one, We two")

$$v_1 = h_{ie} i_1 + h_{re} v_2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

$$i_2 = h_{fe} i_1 + h_{oe} v_2 \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Using these equations, one can obtain expressions for the current gain, voltage gain, input impedance, output impedance and the power gain.

(i) *Current gain* A_i

By definition, the current gain $A_i = \dfrac{i_2}{i_1}$

Putting the value of i_2 from equation (2),

$$A_i = \frac{h_{fe} i_1 + h_{oe} v_2}{i_1} = h_{fe} + h_{oe}\left(\frac{v_2}{i_1}\right).$$

But $v_2 = -i_2 R_L$ (current through R_L is opposite to the direction of i_2)

$$\therefore A_i = h_{fe} + h_{oe}\left(\frac{-i_2}{i_1} R_L\right)$$

$$= h_{fe} - h_{oe} . A_i . R_L$$

$$\therefore A_i(1 + h_{oe}R_L) = h_{fe}$$

$$\therefore A_i = \frac{h_{fe}}{(1 + h_{oe}.R_L)} \quad \ldots\ldots (3)$$

This shows that the current gain A_i is less than h_{fe} and this is due to the presence of the load R_L.

(ii) *Voltage gain* A_v

By definition, $A_v = \frac{v_2}{v_1}$. Putting the value of v_1 from equation (1),

$$A_v = \frac{v_2}{(h_{ie}i_1 + h_{re}v_2)} = \frac{-i_2.R_L}{h_{ie}i_1 + h_{re}(-i_2R_L)} \quad \text{But } v_2 = i_2R_L$$

$$A_v = \frac{-i_2R_L}{h_{ie}i_1 - i_2h_{re}R_L} = \frac{-R_L}{h_{ie}(i_1/i_2) - h_{re}R_L}$$

$$= \frac{-R_L}{(1/A_i) - h_{re}R_L} \quad \text{From the equation (3)}$$

$$A_v = \frac{-R_L}{h_{ie}\left(\frac{1 + h_{oe}R_L}{h_{fe}}\right) - h_{re}R_L} \qquad A_i = \frac{h_{fe}}{(1 + h_{oe}R_L)}$$

$$= \frac{-h_{fe}.R_L}{h_{ie}(1 + h_{oe}R_L) - h_{fe}h_{re}R_L} \qquad \therefore (1/A_i) = \frac{(1 + h_{oe}R_L)}{h_{fe}}$$

$$A_v = \frac{-h_{fe}.R_L}{h_{ie} + R_L\Delta} \qquad \text{Where } \Delta = \begin{vmatrix} h_{ie} & h_{fe} \\ h_{re} & h_{oe} \end{vmatrix}$$

The negative sign shows that the input and the output are 180° out of phase.

(iii) Input impedence Z_i

by definition $Z_i = \frac{v_1}{i_1}$. Substituting for v_1 from equation (1),

$$Z_i = \frac{h_{ie} i_1 + h_{re} v_2}{i_1}$$

$$= h_{ie} + h_{re} (v_2 / i_1)$$

$$= h_{ie} - h_{re} (i_2 / i_1) R_L$$

$$= h_{ie} - h_{re} \cdot A_i \cdot R_L$$

But $v_2 = - i_2 R_L$

But $A_i = \frac{h_{fe}}{(1 + h_{oe} R_L)}$

$$\therefore Z_i = h_{ie} - \frac{h_{re} \cdot h_{fe} \cdot R_L}{(1 + h_{oe} R_L)}$$

The presence of the load R_L has caused a decrease in the input impedance.

(iv) Output impedance, Z_o

By definition, $Z_o = \frac{v_2}{i_2}$ with the signal source voltage shorted ($v_s = 0$).

Putting the value of i_2 from equation (2),

$$Z_o = \frac{v_2}{(h_{fe} i_1 + h_{oe} v_2)}$$

To find, i_1, we use Kirchoff's laws for the input side with the source shorted.

$$\therefore i_1 R_s + i_1 h_{ie} + h_{re} v_2 = 0$$

$$i_1 (R_s + h_{ie}) = - h_{re} v_2$$

$$\therefore i_1 = \frac{- h_{re} \cdot v_2}{(R_s + h_{ie})}$$

Using this value in equation (4),

$$Z_o = \frac{v_2}{h_{fe} \cdot \left(\frac{- h_{re}}{R_s + h_{ie}} \right) + h_{oe} v_2}$$

$$\therefore Z_0 = \frac{(R_s + h_{ie})}{h_{oe}(R_s + h_{ie}) - h_{fe}\,h_{re}}$$

When the source resistance R_S is negligibly small, $R_S = 0$. Then,

$$Z_0 = \frac{h_{ie}}{h_{oe}h_{ie} - h_{fe}h_{re}}$$

$$Z_0 = \frac{h_{ie}}{\Delta} \qquad \text{where } \Delta = \begin{vmatrix} h_{ie} & h_{fe} \\ h_{re} & h_{oe} \end{vmatrix}$$

(v) Power gain, P

$$P = \frac{\text{a.c power output}}{\text{a.c. power input}}$$

$$P = |A_v| \times |A_i|$$

Placing the value of the magnitude of A_v and A_i,

$$\text{Power gain } P = \frac{h_{fe}}{(1 + h_{oe}R_L)} \times \frac{h_{fe}R_L}{h_{ie} + R_L(h_{ie}h_{oe} - h_{re}h_{fe})}$$

In actual practice, h_{oe}, h_{re} are very small quantities. $h_{oe} < 1$ and $R_L\Delta < h_{ie}$

$$\therefore P = h_{fe} \times \frac{h_{fe}R_L}{h_{ie}}$$

$$\therefore P = \frac{h^2_{fe} \cdot R_L}{h_{ie}}$$

This gives the power gain of the C E amplifier, in terms of h parameters.

Note: 1. The ratio (h_{fe}/h_{ie}) is known as the transconductance g_m of the transistor. It is also known as the 'figure of merit' of the transistor.

$$g_m = h_{fe}/h_{ie}$$

2. For CB and CC amplifiers, the above expressions hold good; but the second subscript is replaced correspondingly by b or c instead of e.

Example

Analysis of a transistor CC amplifier, using *h* parameters

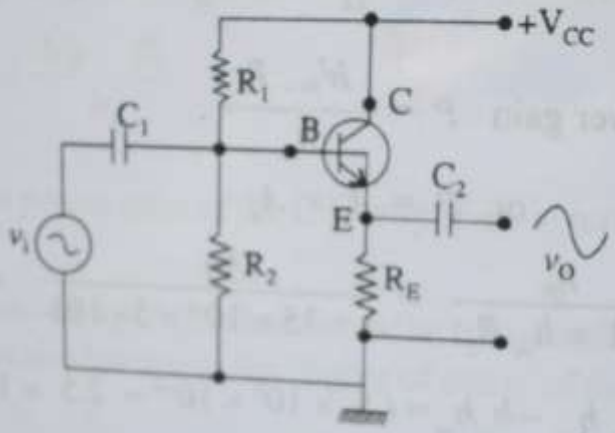


Fig. 118

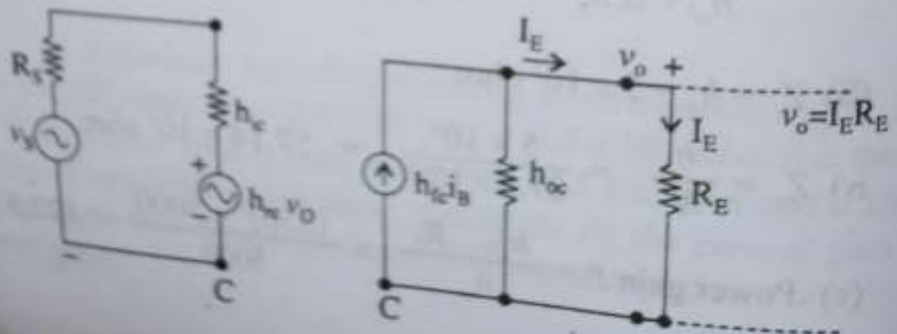


Fig. 119

The circuit diagram of a common-collector *n p* n-transistor amplifier is shown in figure. The input v_i is applied between base and emitter. The output is drawn across R_E in the emitter circuit. The output is in phase with the input wave. The common collector *h* parameter *a.c.* equivalent is drawn by replacing the transistor with a voltage generator that generates a voltage $(h_{re} v_o)$ in series with the input impedance (h_{ie}) and a current generator that generates a current $(h_{fe} i_b)$ parallel to the output admittance (h_{oe}). The source voltage is v_i and its resistance is R_s as marked in the equivalent circuit. The load R_L is actually the emitter resistance R_E, from which the output v_o is obtained.

1. *To calculate input impedance of the CC amplifier*

For simplicity we assume that here, the reverse voltage transfer ratio to be = 1. Looking at the input part of the equivalent circuit.

$$v_i = i_b h_{ie} + v_o . 1$$
$$= i_b h_{oe} + i_E R_E \quad \text{since } v_o = i_E R_E$$

$= i_b h_{ic} + h_{fe} i_b \cdot R_E$ since $h_{fe} = \frac{i_E}{}$

$= i_b (h_{ic} + h_{fe} \cdot R_E)$.

The inpupt impedance $Z_i = Z_b$

$= \frac{v_i}{}$

$\therefore Z_i = h_{ie} + h_{fe} R_E$

2. *To calculate the output impedance*

The output impedance $A_0 = Z_E$ when the signal voltage is zero.

$$Z_E = \frac{v_o}{i_b} \quad \text{.... .... (1)}$$

Now i_E can be expressed in terms of v_o. Looking at output part of the circuit,

$$i_E = h_{fe} \cdot i_b \quad \text{..... ..... (2)}$$

Now, from input part of the circuit,

$$i_b h_{ic} = h_{re} \cdot v_o \quad \text{for input short circuited } (v_s = 0)$$

$$= 1 \times v_o$$

$$\therefore i_b = \frac{v_o}{h_{ic}}$$

To be more accurate, the source resistance R_s can be added to h_{ic}.

$$\therefore i_b = \frac{v_0}{(h_{ic} + R_s)}$$

Putting this in equation (2),

$$i_E = h_{fe} \cdot i_b$$

$$i_E = \frac{h_e \cdot v_o}{(h_{ie} + R_s)}$$

Using this value in equation (1).

$$Z_E = \frac{v_o}{i_E}$$

$$= \frac{v_o (h_{ic} + R_s)}{1 + h_{oe} R_E}$$

$$Z_E = \frac{(h_{ic} + R_s)}{h_{fe} \cdot v_o}$$

Now, actually $Z_0 = Z_E \,//\, R_E$

Since the load R_E is much larger than Z_E, we can take $Z_0 = Z_E$

Thus, the output impedance of the amplifier is

$$Z_0 = \frac{(h_{ic} + R_s)}{h_{fe}}$$

3. *To calculate the voltage gain* A_v

$$A_v = \frac{v_o}{v_i}$$

Now,. $v_o = i_E \, R_E$ for the output .... (3)

$$v_o = h_{fc} i_b . \, R_E$$

i_b can be expressed in terms of v_i and v_o. Looking at the input circuit,

$$v_i = v_0 + h_{ic} . \, i_b$$

$$\therefore \quad \frac{(v_i - v_o)}{h_{ic}} = i_b .$$

Putting this in equation (3),

$$v_o = h_{fe} \, R_E \, \frac{(v_i - v_o)}{h_{ic}}$$

$$\therefore \quad h_{ic} . v_0 = h_{fe} R_E v_i - h_{fc} R_E v_o$$

$$\therefore \quad v_o (h_{ic} + h_{fc} R_E) = h_{fc} R_E . v_i$$

Dividing throughout by h_{ic},

$$v_o \left(1 + \frac{h_{fe} R_E}{h_{ic}}\right) = \frac{h_{fe}}{h_{ic}} . \, R_E \, v_i$$

Hence, the voltage gain $A_v = \frac{v_o}{v_i}$

$$A_v = \left(\frac{h_{fc} R_E}{h_{ic}}\right) \times \frac{1}{\left(1 + \frac{h_{fc}}{h_{ic}} \cdot R_E\right)}$$

$$A_v = \left(\frac{h_{fc} R_E}{h_{ic}}\right) \times \frac{1}{\left(\frac{h_{fc} \cdot R_E}{h_{ic}}\right)} \quad \text{since} \quad \frac{h_{fc}}{h_{ic}} \cdot R_E \gg 1$$

$\therefore A_v = 1$

4. *To calculate the current gain*

From the output circuit, generator current

But $v_o = i_E \cdot R_E$

$$h_{fc} \cdot i_B = h_{ic} \cdot V_o + i_E$$

$$\therefore h_{fc} \cdot i_B = h_{oc} i_E R_E + i_E$$

$$h_{fc} \cdot i_B = i_E (1 + h_{oc} R_E)$$

$$\therefore \frac{i_E}{i_B} = \frac{h_{fc}}{(1+h_{oc} R_E)}$$

*i.e.*the current gain of the amplifier is

$$A_i = \frac{i_E}{i_B} = \frac{h_{fe}}{(1+h_{oc} R_E)}$$

Since $R_E = R_L$, the load from which the output is taken.

$$\therefore A_i = \frac{h_{fc}}{(1 + h_{oc} R_L)}$$

4. *To calculate the current gain*

From the output circuit, generator current

$$h_{fc}.\, i_B = h_{ic}.V_o + i_E \qquad \text{But } v_o = i_E .\, R_E$$

$$\therefore h_{fc}.\, i_B = h_{oc}\, i_E\, R_E + i_E$$

$$h_{fc}.\, i_B = i_E (1 + h_{oc}\, R_E)$$

$$\therefore \frac{i_E}{i_B} = \frac{h_{fc}}{(1+h_{oc} R_E)}$$

*i.e.*the current gain of the amplifier is

$$A_i = \frac{i_E}{i_B} = \frac{h_{fe}}{(1+h_{oc} R_E)}$$

Since $R_E = R_L$, the load from which the output is taken.

$$\therefore A_i = \frac{h_{fc}}{(1 + h_{oc} R_L)}$$

Analysis of common base trnsistor amplifier

CB amplifier circuit diagram is re-drawn for the purpose of drawing its *h* - parameter equivalent circuit.

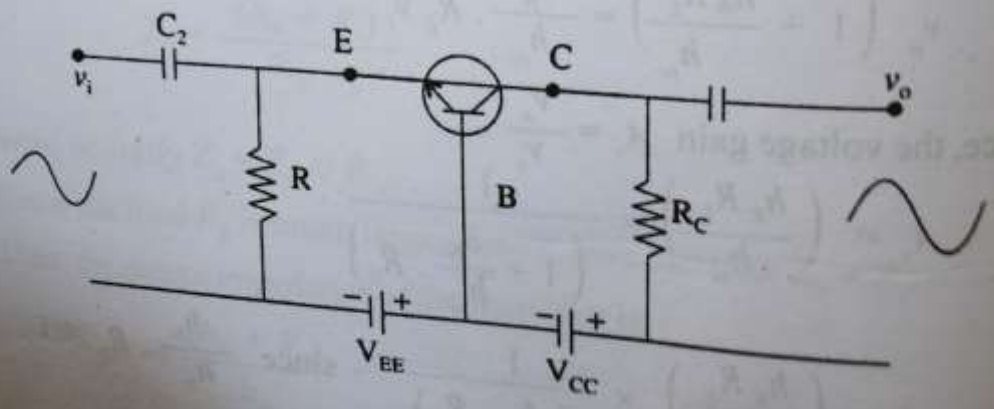


Fig. 120

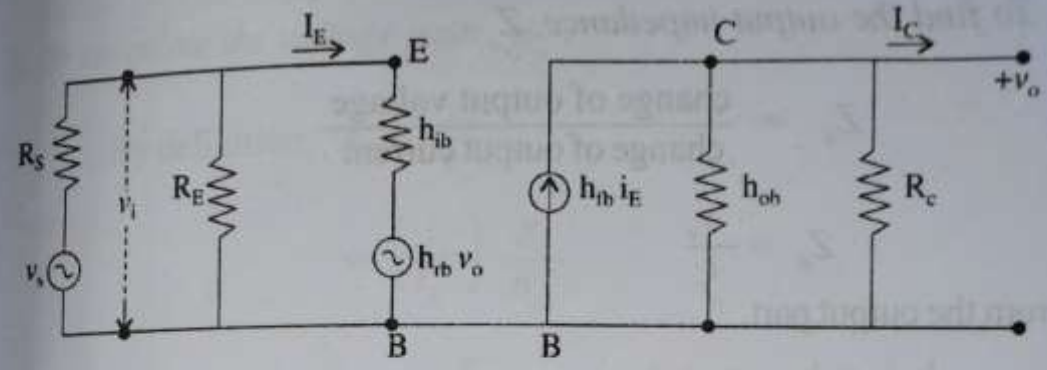


Fig. 121

The h-parameter equivalent circuit of a CB amplifier consists of input part and output part connected through ground. The input part consists of a voltage generator that generate a voltage $(h_{rb}.v_o)$ in series with the input impedance (h_{ib}) of the transistor, parallel to the resistance in emitter circuit, R_E. The output part consists of circuit generator that generates a current $(h_{fb}.i_E)$, parallel to the output admittance (h_{ob}) of the transistor. The load resistance R_c is in parallel to (h_{ob}). The output voltage v_0 is available across R_c. The input and output currents are I_E and I_c respectively, as marked in the diagram.

1. To calculate input impedance

By definition.

$$\text{Input impedance } Z_i = \frac{\text{change of input voltage}}{\text{change of input current}}$$

$$= \frac{v_o}{i_E}$$

$$= \frac{v_i}{\frac{v_i}{(h_{ib} \,//\, R_E)}}$$

$$= h_{ib} \,//\, R_E$$

$$\therefore Z_i = h_{ib} \qquad \text{since } R_E >> h_{ib}.$$

2. *To find the output impedance, Z_o*

$$Z_0 = \frac{\text{change of output voltage}}{\text{change of output current}}$$

$$Z_0 = \frac{v_o}{i_c}$$

From the output part,

$$h_{fb} i_E = h_{ob} \cdot v_o + i_c$$

$$\therefore i_c = h_{fb} \cdot i_E - h_{ob} \cdot v_o \quad \ldots\ldots (1)$$

Considering the shor-circuited input part of the equivalent circuit (for finding Z_0 by definition),

$$i_E h_{ib} - h_{rb} v_o = 0$$

$$i_E = \frac{h_{rb} \cdot v_o}{h_{ib}}$$

Putting this value in equation (1).

$$i_c = h_{fb} \cdot \frac{h_{rb} v_o}{h_{ib}} - h_{ob} v_o$$

$$= v_0 \left(\frac{h_{fb} i_{rb}}{h_{ib}} - h_{ob} \right)$$

$$= \frac{v_o}{h_{ib}} (h_{fb} h_{rb} - h_{ob} h_{ib})$$

$$i_C = \frac{v_o \cdot \Delta}{h_{ib}} \qquad \text{where } \Delta = \begin{vmatrix} h_{fb} & h_{ib} \\ h_{ob} & h_{rb} \end{vmatrix}$$

$$\therefore \frac{v_o}{i_C} = \left(\frac{h_{ib}}{\Delta} \right)$$

$\therefore$ output impedance $Z_0 = \frac{v_0}{i_C}$

$$Z_0 = \frac{h_{ib}}{\Delta}$$

3. *To calculate the voltage gain* A_v

By definition, $A_v = \frac{v_o}{v_i}$

$$= \left(\frac{i_c}{i_E}\right) \frac{R_c}{h_{ib}}$$

$$A_v = h_{fb} \cdot \frac{R_c}{h_{ib}}$$

This is a positive quantity.

∴ The output signal voltage is in phase with the input signal voltage.

4. *To calculate the current gain* A_i

By definiton, $A_i = \frac{i_c}{i_E}$

From the output port,

$$h_{fb} i_E = v_o \cdot h_{ob} + i_c$$

$$\therefore i_c = h_{fb} i_E - v_o \cdot h_{ob}$$

$$i_c = h_{fb} i_E - R_c i_c h_{ob} \quad \text{since } v_o = R_c i_c$$

$$\therefore i_c(1 + h_{ob} \cdot R_c) = h_{fb} \cdot i_E$$

$$\therefore \frac{i_c}{i_E} = \frac{h_{fb}}{(1 + h_{ob} \cdot R_c)}$$

$$\text{i.e., } A_i = \frac{h_{fb}}{(1 + h_{ob} \cdot R_c)}$$

5. *To calculate the power gain, P*

Power gain = current gain × voltage gain

$$P = A_i \times A_v$$

Since A_i and A_v are known, the power gain can be calculated.

Common emitter Transistor amplifier (R.C. coupled) amplifier

(i) *Circuit and functions of the components*

A common emitter transistor amplifier circuit with *n-p-n* transistor is shown in the figure. R_C is the load resistance in the collector circuit. The resistance R_1 and R_2 form the potential divider arrangement, which is used to give bias to the base from the supply voltage V_{CC}. R_E is a resistance

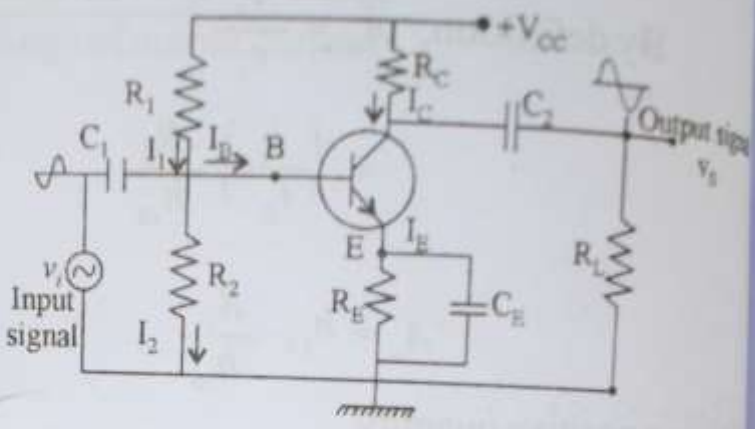


Fig.122

connected in the emitter circuit to compensate for the variation of the collector current due to any temperature change. The base bias may also alter due to a.c. flowing through resistance R_E. To eliminate this variation of voltage across R_E, the capacitance C_E is connected parallel to R_E. This capacitor is known as a.c. by - pass capacitor. C_1 is a capacitor used to couple the signal to the base of the transistor. This will prevent d.c. of the power supply to enter into the input source. It allows only the a.c. signal to be applied between the base and emitter. C_2 is the coupling capacitor which makes only the a.c. voltage available at the output terminal with respect to the ground, across the load resistance R_L (next stage).

(ii) *biasing*

The resistances R_1, R_2 and R_E form the biasing circuit. The biasing circuit components are so chosen that the desired operating point (namely V_{CE} and I_C values) is obtained to ensure the output voltage without any distortion i.e., a faithful amplifier output is like the input signal shape.

(iii) *Input capacitor*

C_1 is the input capacitor. It is an electrolytic capacitor of about 10 μF value. This couples the signal voltage to the base of the transistor. In the absence of C_1, the signal source gets directly connected to the base, changing the biasing condition. C_1 allows only a.c. signal to flow to the base, but isolates the signal source from R_2.

(iv) *Emitter by-pass capacitor* C_E

The capacitor C_E is connected parallel to the emitter resistor R_E, in order to by-pass a.c. signal through it. This prevents any a.c. voltage drop across R_E. The reactance $\left(X_C = \frac{1}{C\omega} \right)$ of the by-pass capasitor should be small, sompared with R_E for by-pass action. This means, the capacitor C_E should have large value (100 μF). The presence of C_E also avoids any fluctuation of gain of the amplifier, resulting in stability of amplifier functioning.

(v) *Coupling capacitor* C_2

The capacitor C_2 is of low value like 10 μF. It couples the output a.c. signal to the load. The coupling capacitor also prevents d.c. current to flow from the collector to the load. Since only a.c. output signal is coupled to the load due to the presence and action of R_C and C_2, the amplifier is called R.C. coupled amplifier.

(vi) *Various circuit currents*

(a) *Base current:* When no signal is applied to the base circuit, the d.c. base current is I_B. When a.c. signal input is applied, the a.c. base current i_b also flows.

∴ The total base current $i_B = I_B + i_b$.

(b) *Collector current:* When no signal is applied, a d.c. collector current I_C flows due to biasing circuit. When a.c. signal is applied, the a.c. collector current i_c also flows.

∴ The total collector current $i_C = I_C + i_c$

By definition of β,

$I_C = \beta I_B$ = zero signal collector current

$i_C = \beta i_b$ = collector current due to the applied signal.

(c) *emitter current:* When no signal is applied a d.c. emitter current I_E flows. With the application of input signal,

total emitter current $i_E = I_E + i_e$

Now, $I_E = I_B + I_C$ due to transistor action.

Also, $i_e = i_b + i_C$

The base currents are very small.

$\therefore \quad I_E = I_C$

$i_e = i_c$

(vii) *Working of the amplifier*

The input a.c. signal is applied to the base with respect to the ground and the output signal appears across the load R_C at the collector. This output signal is then passed through coupling capacitor C_2 to the next stage. The input signal either aids or opposes the base-emitter-bias. When it aids the base, the base current I_B goes up because the emitter-base voltage is increased due to higher forward bias. Hence, collector current increases and so the voltage drop across R_C is more. Therefore, the voltage at the collector (output) decreases. Thus when the input signal increases, the output voltage decreases.

The opposite happens, when the input signal goes down. Thus there is phase change of 180° (π radian) in the output voltage when compared to the input signal.

We have seen that the effect of the increasing input signal is to produce a small increase in the base current. This causes a large increase of collector current due to the transistor action. Such large variation of collector current occuring in a large resistance (the load) produces a very large voltage drop across it and this is the output. Thus the weak signal is amplified as a large output voltage.

The transistor itself does not produce the larger output voltage. It draws power from the battery V_{CC} and only regulates the current flow through it such that the output voltage is large.

Phase change

The input and output voltages are 180° out of phase as shown in the circuit diagram. This can be proved as follows: According to the load line equation,

$V_{CC} = I_C R_C + V_{CE} + I_E R_E$.

Differentiating, $0 = dI_C R_C + dV_{CE} + 0$ since there is no variation of current through R_E due to the presence of the by-pass capacitor.

$$\therefore\ dV_{CE} = -dI_C.R_C$$

The variation dI_C follows the input voltage variation. So, the output (dV_{CE}) has a phase shift π of with respect to the input, as shown by the negative sign in the above equation.

Voltage gain of the amplifier

The effective a.c. load to the amplifier is $R = R_C \,||\, R_L$

The output voltage $v_o = i_C \times R$

The input resistance $= R_i$

Input voltage $v_i = i_b \times R_i$

Voltage gain $A_v = \dfrac{v_o}{v_i}$

$$= \frac{i_C}{i_b} \times \frac{R}{R_i}$$

$$A_v = \beta . \frac{R}{R_i}$$

Knowing the input resistance (R_i) of the amplifier, the voltage gain can be calculated.

Power gain $P = \dfrac{i_C^2 . R}{i_b^2 R_i}$

$$R = \frac{R_C R_L}{R_C + R_L}$$

$$P = \beta^2 . \frac{R}{R_i}$$

Main features of the CE amplifier

1. It has low voltage and power gain.
2. The current gain is large.
3. The input and output signals are 180° out of phase with each other.
4. The input impedance is low. ($r_e = \beta$).
5. The output impedance is high.

6. The frequency response of RC amplifier provides constant gain over a wide range; hence. most suitable for audio applications.

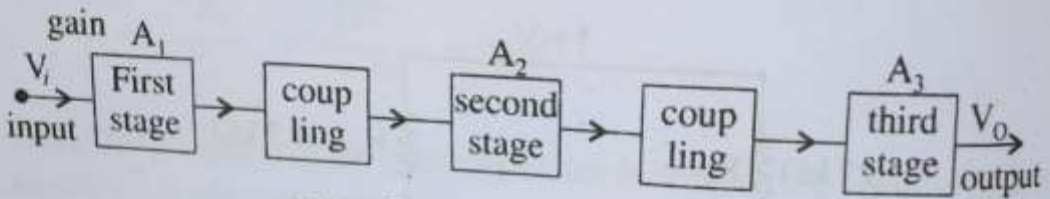
As the voltage gain and the current gain are large, the CE amplifiers are used in many variety of applications. Amplifiers are used in wireless communications and broadcastings and in audio equipment of all kinds.

'*Input impedance*' of an amplifier is the ratio of the *change* of input voltage to the *change* of input current supplied by the source.

'*Output impedance*' of an amplifier is the ratio of the *change* of output voltage to the *change* of output current supplied to the load.

Multistage Transistor Amplifier

A transistor circuit containing more than one stage of amplification is known as multistage transistor amplifier.



over-all gain $A = A_1 \times A_2 \times A_3$

Fig. 124 Block diagram of multistage (3 stage) amplifier

The output of first -stage is connected to the input of second stage through a suitable coupling device. The coupling, may be RC coupling, transformer coupling or direct coupling. The output impedance of first stage may not be equal to the input inpedance of second stage. This will affect the net amplification. Inpedance matching is done by the coupling device such as a transformer.

In a RC coupled amplifier the input impedance of second stage is low while the output inpedance of first stage is high. When they are coupled to make a multistage amplifier, the high output inpedance of the first stage comes in parallel with the low input inpedance of next stage. Hence the effective load resistance is decreased. This is the reason for

low voltage gain of first stage and low power gain of the RC coupled amplifier. This problem can be overcome by transformer coupled amplifier. In a transformer coupled amplifier the stages are coupled using a transformer. The overall gain of a multistage amplifier is the product of the gains of the individual stages.

Gain $A = A_1 \times A_2 \times A_3 \times$ ----------

Transformer coupled amplifier

In transformer coupled amplifier, a transformer is used to transfer the output voltage of the first stage to the input of the second stage. The primary winding of the transformer is in the transistor collector circuit (in the place of R_C) of first stage. One end of the secondary coil is connected directly to the base of transistor T_2 in the second stage, whereas the other end is connected to the middle of the potential divider. formed by R_3 and R_4 of the biasing circuit for T_2 as shown in the diagram.

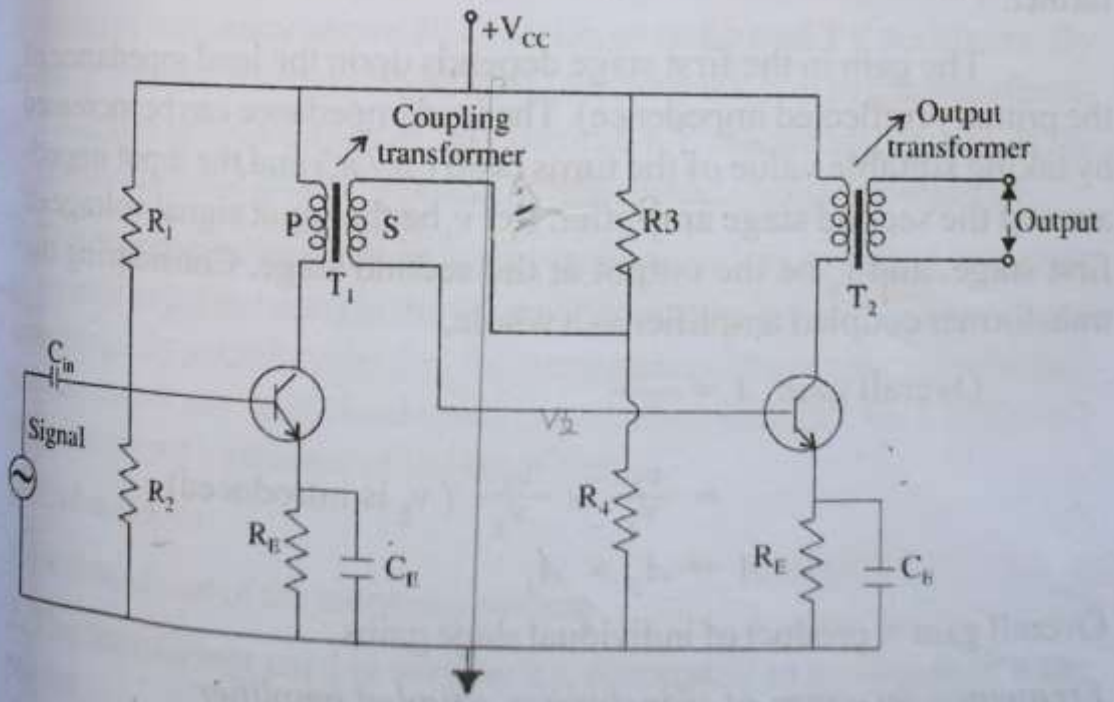


Fig. 125 Transformer coupled amplifier

The input signal voltage v_s is applied to the base of T_1. The output can be drown from the secondary coil of the output transformer in T_2.

The two stages are isolated by the use of the transformer coupling. There is no path for current flow from primary to the secondary coil of the transformer in T_1. However. the voltage variations in the primary cause induced voltage in the secontary, depending on the turns rat (n_1/n_2) of the transformer.

$\frac{v_2}{v_1} = \frac{n_2}{n_1}$ where suffux 1 is for primary side and suffux 2 is for secondary side.

$$v_2 = \left(\frac{n_2}{n_1}\right) \times v_1$$

Moreover the current variations in the collector circuit do not dissipate power much as there is no resistance with collector circuit. The output of the transformer is applied to the base of the second stage as shown in the diagram, without loss of voltage. The second amplifier amplifies the signal further.

The gain in the first stage depends upon the load inpedance of the primary (reflected impedence). The load impedance can be increased by taking suitable value of the turns ratio (n_1/n_2) and the input impedance of the second stage amplifier. Let v_1 be the input signal voltage of first stage. and v_0 be the output at the second stage. Considering the transformer coupled amplifier as a whole,

Overall gain $A = \frac{v_0}{v_1}$

$$= \frac{v_2}{v_1} \times \frac{v_0}{v_2} \quad (v_2 \text{ is introduced})$$

$$A = A_2 \times A_1$$

Overall gain = product of individual stage gains

Frequency response of transformer coupled amplifier

The gain of the amplifier is constant only for a small range of frequencies.

The output voltage = collector current × reactance of primary.

At low frequencies. the reactance of primary begins to fall, resulting in decreased gain. At high frequencies, the capacitance between turns of winding acts as a bipass capacitor to reduce the output voltage and the gain is decreased. So there is frequency distortion in this amplifier. The frequency response curve of transformer coupled amplifier is shown in figure.

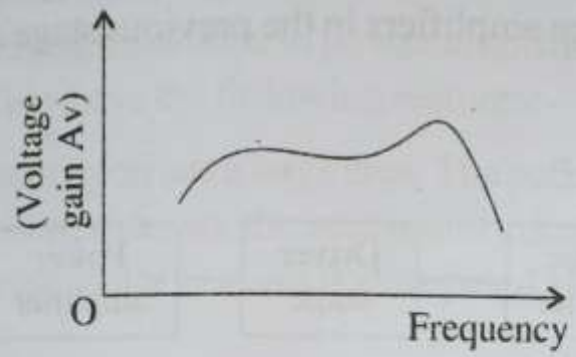


*Fig.*126

Advantages

1. Transformer coupled amplifer are widely used for amplification of *r.* signals (of frequency above 20 kHz) i.e. in radio and TV receivers. By putting suitable shunting capacitors across each coil in the transformers, one can get resonance at any desired r. f. frequency, by adjusting the capacitors. Such amplifiers are called turned - voltage amplifier.

2. This coupling scheme not only prevents power loss in the collector due to resistor being not used in the circuit but also helps proper impedance matching. By suitably selecting the turns ratio of the output transformer, we can match any load (loud speaker coil resistance 3Ω,10Ω, 80Ω etc.) with the output inpedance of the amplifier.

Disadvantages

1. Increased size of the amplifier system

2. The transformer used is very bulky, compared to a resistor or a capacitor

3. The transformer used differs from an ideal one. There is some leakage inductance and interwinding capacitances. Because of these stray elements, the amplifier does not amplify signals of all frequencies equally well.

Transistor audio power amplifier

The amplifier driving loud speaker in the output section of a radio receiver is an example of power amplifier. In a power amplifier, both voltage magnification and current amplification have to take place. Actually the input voltage, before being applied to power amplifier, is amplified to high level by voltage amplifiers in the previous stage as shown in the block diagram.

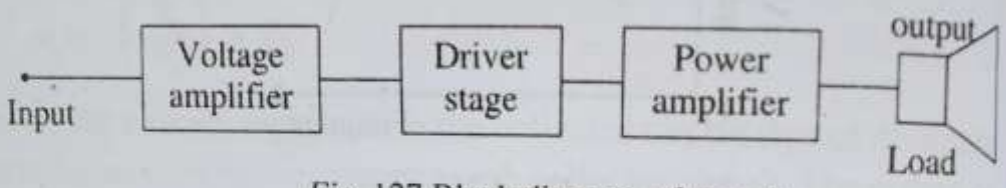


Fig. 127 Block diagram of transistor audio power amplifier

As regards current amplification, power transistors are used to handle large collector current swing. The resistance in the collector circuit will then dissipate power. To minimise such power dissipation, the resistor in the collector circuit is replaced by inductance coil (or choke) such as the primary coil of a transformer. The choke dissipates lesser power. The schematic arrangement of a power amplifier is given here. An audio power amplifier handles signals in the range 20 to 20 thousand hertz frequency.

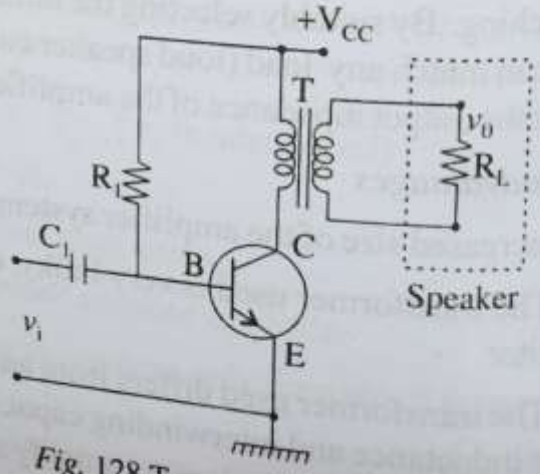


Fig. 128 Transistor power amplifier

A power amplifier actually takes power from the supply and delivers it as useful signal power to the load, raising the power level.

The ratio of signal power delivered as output to

c. power input is known as the efficiency of the power amplifier. The fficiency is most important when large amounts of signal power are equired. The power amplifier efficiency is related to how the amplifier is iased. Power amplifiers are classified according to the position of the perating point (Q-point) on the load line.

The transistors used in power amplifiers are known as power ransistors. They have the following features:

. The collector region has a large area. The collector is connected firmly o a metallic heat sink. So, the heat mainly developed in the depletion egion of the transistor is quickly dissipated and safety of transistor is ensured.

2. The emitter and base layers are heavily doped.

Difference between voltage amplifier and power amlifier

Voltage amplifier

Voltage gain $A_v = \beta \times \frac{R}{R_i}$ where β is a.c. current gain of the transistor, R is the effective load resistance, R_i is input resistance of the voltage amplifier. To get high voltage amplification, we have to have β large, R large and R_i small. A transistor with high value of β is to be used.

Power amplifier

Power gain $P = \beta^2 \times \frac{R}{R_i}$

The amplifier has to handle large current. Large current means more heat is produced in the collector. The heat produced must be dissipated. So, the collector is connected firmly to a metallic heat sink. This makes the power transistor large. Moreover, the transistors with smaller β are to be used in power amplifiers. Transformer coupling is used for impedance matching at the output part. In summary, we have the folowing particulars:

Particulars	Voltage amplifier	Power amplifier
1. β	greater than 100	low (5–20)
2. R_C	high (4–10 kΩ)	low (5–20Ω)
3. Coupling	R.C. coupling	Transformer coupling
4. Collector current	low (1mA)	high (100 mA)
5. Power output	low	high
6. Output impedance	high (12 kΩ)	low (20Ω)

Classification of power amplifiers

Power amplifiers handle large signals. The input signals may drive the collector current to cut off or saturation region. The collector current may flow for part of the period of the input a.c. signal and may not flow during the remaining period. So, the power amplifiers are classified according to the portion of the input cycle for which the collector current flows.

Class A power amplifier

It is one in which the current flows for the entire cycle of the input signal. The transistor operates in the active region at all times. The Q-point must be at the middle of the d.c. load line for maximum output signal swing. The output is full cycle each time as shown in figure .

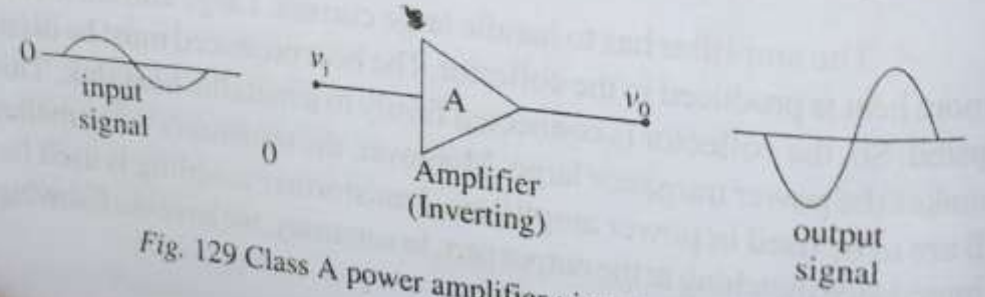


Fig. 129 Class A power amplifier : input - output signal

Class B power amplifier

It is one in which the current flows only during one half cycle of the input signal. The transistor operates in the linear region for half of the input cycle and is cut-off for the other half. The Q- point is at the of value of V_{CE} where ($I_C = 0$). The output is only for half the input cycle as shown in figure.

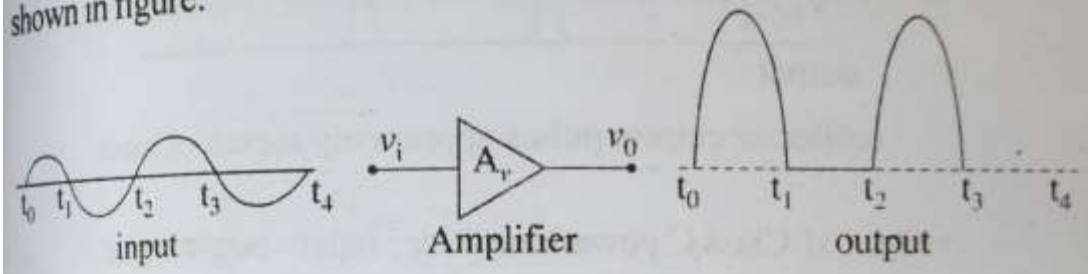


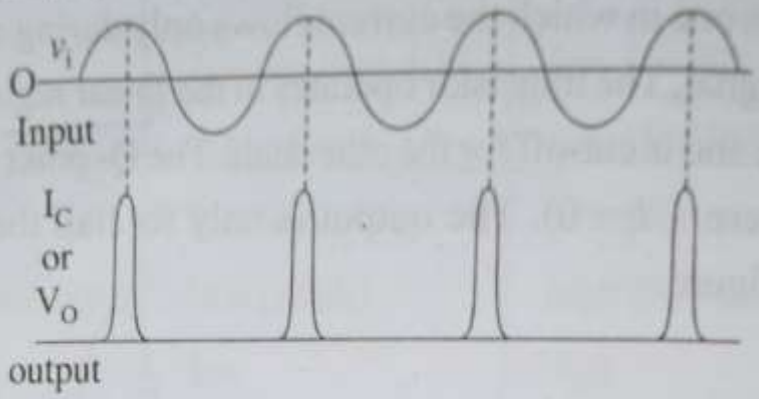
Fig. 130 Class B power amplifier : input - output signal

The class B amplifiers are used in push-pull configuration (two amplifiers - one to amplify one half of the input signal and the other to amplify the other half of the input signal) in order to get output as the replica of input.

Class AB power amplifier

Here the collector current flows for more than half a cycle of the input signal but for less than full cycle. The class AB amplifier is biased slightly above cut-off voltage and operates in the linear region for slightly more than half of the input cycle. The Q-point is near the lower end of the load line. The class AB eliminates cross-over distortion found in class B.

Class C power amplifier



(collector current pulses appear only at peak of input

Fig. 131 Class C power amplifier : input - output signal

It is one in which the collector current flows for less than half a cycle of the input signal. The class C amplifiers is biased slightly beyond (below) cut-off. The efficiency of class C amplifier can be nearly 100%. The class C amplifiers are normally operated as tuned amplifiers to produce powerful sinusoidal output from LC-circuits, used as load. The LC circuits are tuned to a particular selective frequency

Push pull amplifier (Class B power amplifier)

The audio power amplifier used in transistor receivers, tape recorders, record players, PA systems etc make use of the push-pull circuit. Push pull amplifiers have increased power output, efficiency and less distortion.

A combination of two class B amplifiers working together is called push-pull amplifier (fig.).

The push-pull amplifier circuit uses two identical transistors T_1 and T_2 whose emitter terminals are connected together. The circuit uses two transformers one at the input and the other at the output. The input transformer (IT) has a centre-trapped secondary winding. It provides opposite polarity inputs to the bases of the two transistors. The primary of the output transformer (OT) is also centre-trapped. The collector

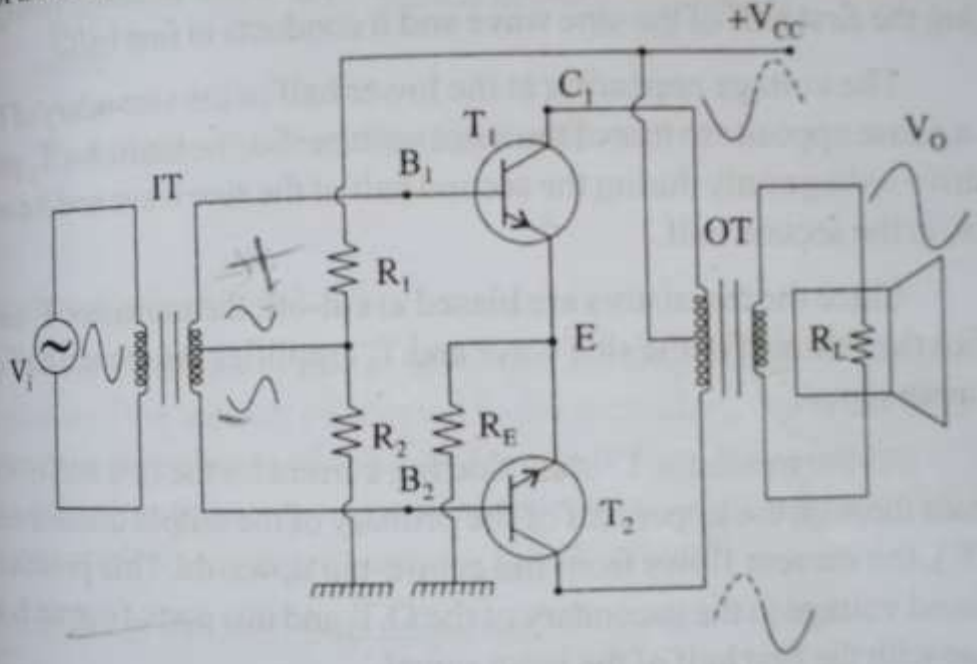


Fig. 134 Push - pull amplifier

terminals of the two transistors are connected to the supply voltage V_{cc} through part of the primary of this transformer. The load R_L (loud speaker, for example) is connected across the secondary of the output transformer. The turns ratio is properly chosen to match the load and output impedance of the transistors. Under well-matched condition, there is maximum power delivered to the load by the amplifier. The resistors R_1, R_2 and the emitter resistance R_E are used to bias the amplifier under class B condition i.e., the operating point is at cut off) so that practically no output current flows in the absence of an applied signal.

Working

The class B amplifier is biased at cut-off. With no signal input, both the transists T_1 and T_2 are cut-off.

When a sine wave voltage is applied as the input across the primary of the input transformer (IT), a sine wave voltage of the same phase appears in the upper half of the secondary of IT. Thus, the input to base of transistor T_1 is a sine wave voltage, which has the same phase as in the input voltage i.e., the transistor T_1 gets the positive voltage during the first half of the sine wave and it conducts in first half.

The voltage appearing at the lower half of the secondary of IT has a phase opposite to that of the input voltage. So, the transistor T_2 gets positive voltage only during the second half of the sine wave and it conducts in the second half.

Since the transistors are biased at cut-off, the transistor T_1 amplifies the first half of the sine wave and T_2 amplifies the second half of the input signal.

As the transistor T_1 is conducting current for the first half of the signals through the upper half of the primary of the output transformer (O.T.), the current flows from the centre-tap upwards. This produces induced voltage in the secondary of the O.T. and this part of output is in phase with the first half of the input signal.

As the transistor T_2 is conducting only during the second half of the signal through the lower half of the primary of the O.T, the current from the centre tap flows downwards. This produces induced voltage in the secondary of the O.T. and this is in phase with the second half of the input signal.

Thus, one complete cycle of the input signal gets power-amplified to produce an output signal which is a replica of the input complete signal.

We see that during one half cycle of the input signal, the circuit pushes the signal high and during the next half cycle, the circuit pulls the

signal low at the output. For this reason, the circuit is called push-pull amplifier.

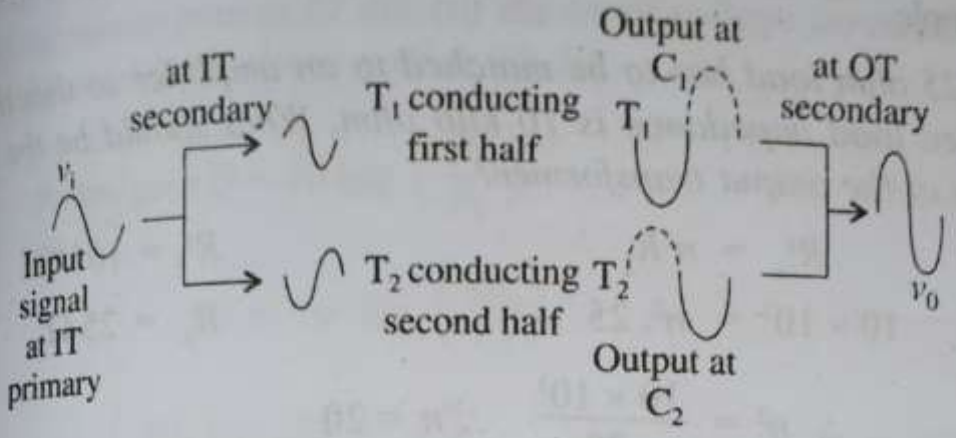


Fig. 135 Working of push pull amplifier

Calculation of a.c. load

Let R' be the a.c. load at the output the amplifier. If R_L is the load resistance of the speaker connected in the secondary, the reflected impedance in the primary of the transformer is $R' = n^2 R_L$ where n is the turns ratio of the transformer. n = number of turns in the primary divided by number of turns in the secondary. This R' gives the a.c. load.

Advantages of the push pull amplifier

1. The output is true replica of the input signal.
2. The d.c. components of the collector current in the output transformer are in opposite directions. This prevents the transformer core from getting into saturation (beyond which output may not vary as input) in the transformer.
3. Higher efficiency with less distortion can be secured with the class B push-pull amplifier. The maximum efficiency = 79%.
4. There will be no hum in the amplifier output, since the ripple currents due to power supply flow in opposite directions in the output transformer.

5. There is no current drain, when the signal is zero. ie; no current flow in the OT primary when there is no input signal.

Field effect transistor (FET)

The field effect transistor is a semiconducting device in which the output current is controlled by an electric field. Since the current is carried by one type of charge carriers, (electron or hole) especially the majority carriers., the FET is also called a unipolar transistor (single carrier type operation). The main difference of BJT and FET is that BJT is current controller device and FET is voltage contoller device. FETs are of two types:

(i) the junction field effect transistor (JFET) and

(ii) the metal oxide field effect transistor (MOSFET).

Structure of a JFET

Figure shows a junction field effect transistor. It consists of a uniformly doped semiconductor bar called a channel. The semi-conductor may be of *n*-type material or of *p* - type material. In the former case, it is called *n*-channel JFET and in the latter case, it is called p-channel JFET. It has two terminals at its end one is called the source (S) and the other is called the drain (D).

A gate (G) is formed by placing a ring of *p* material around the centre of the *n* channel to form a *p-n* junction between the channel and the gate. A depletion region is formed at the *p-n* junction.

Current is allowed to flow along the length of the bar, by applying a voltage between the end terminals D and S of the bar. The current is carried by the majority carriers which drift through the channel. Silicon and sometimes gallium arsenide are taken as the basic semi-conductors for the JFETs.

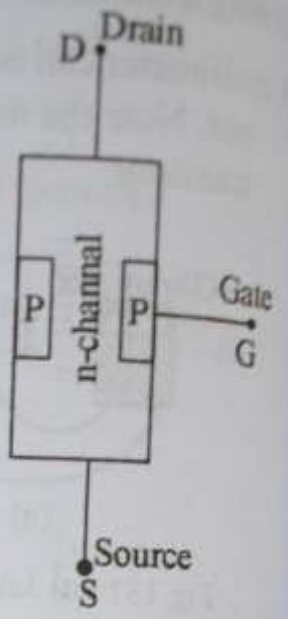


Fig. 138 *Structure of JFET.*

Source (S): It is a terminal through which the majority carriers enter the channel region.

Drain (D) : It is a terminal through which the majority carriers leave the channel.

Gate (G) : Heavily doped region formed surrounding the semiconductor at the middle, with impurities opposite to that of the channel.

The circuit symbols of *n*-channel and *p*-channel JFETs are shown in figure 133. Notice that the arrow on the gate points 'in' for *n*-channel and 'out' for *p*-channel.

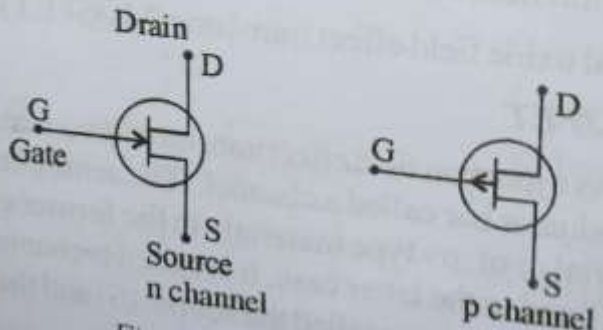


Fig. 139 *Circuit symbol of JFET.*

The arrow on the gate terminal shows the direction of the gate current, when the gate - source junction is forward biased. (The arrow is simply from *p* to *n* material as in a diode).

Principle and Working of a JFET

An *n*-channel JFET, with its terminals properly connected to the voltage sources, is shown in the fig. The drain is given a positive voltage (V_{DD}) with respect to the source to give the reverse bias at the *pn* junction. ie; reverse bias at gate – channel junction.

1. With $V_{GS} = 0$, the majority carriers of the channel drift along the channel to reach the drain due to V_{DD}. The depletion region in the channel near the gate is small and the channel width is wider. Hence the drain current is determined by the channel resistance and V_{DD}.

2. When a negative voltage is applied to the gate, thus reverse biasing the gate, the depletion region will extend into the channel and it becomes wider at the top. Hence the channel becomes narrow. The channel is narrower near the drain, because of the potential gradient along the bar. The depletion region contains no mobile charges and no free carriers. The size of the depletion layer determines the width of the conducting channel. The more negative the gate voltage is, the narrower the channel becomes. Thus, for a given drain-to-source voltage, the drain current will be a function of the gate-to-source voltage. In other words, the gate voltage *controls* the current between the source and the drain.

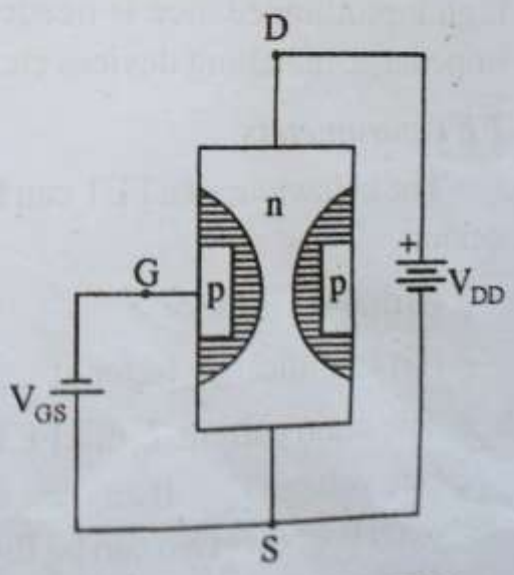


Fig. 140 Working of a JFEJ

3. As the gate voltage is more and more negative, the drain current becomes smaller and smaller.

4. As the gate voltage becomes more and more positive, the drain current becomes larger and larger. The result is that a small change in voltage at the gate produces a large change in drain current. Thus JFET acts as an amplifying device.

The name field effect is used for the FET device since *the field* introduced by the gate *controls* the channel conductance and hence the *device current*.

Input impedance of FET

When V_{GS} is negative, the *p-n* junction is reverse biased. The current drawn by the gate is extremely small. In other words, the input impedance between the gate and the source of a junction FET is very large. It is of the order of megohm. That is why JFET is preferred in devices where high inptut impedance is needed. Example: amplifiers, voltmeters, impedance matching devices etc. This shows the importance of JFET.

FET parameters

The behaviour of a FET can be defined by a set of parameters given below:

(i) drain resistance, r_d (ii) transconductance, g_m

(iii) amplification factor, μ

The drain current I_D in a FET depends on the drain voltage V_{DS} and the gate voltage V_{GS}. If any one of these three is kept fixed, the relation between the other two can be found. These relations help us to define the above parameters of the FET.

(i) The drain resistance of a FET is the ratio of the small change in drain voltage to the resulting change in the drain current at constant gate voltage.

$$r_d = \left(\frac{\partial V_{DS}}{\partial I_D}\right)_{V_{GS}} \text{ohm.}$$

(ii) The transconductance of a FET is the ratio of the small change in the drain current to the corresponding change in the gate-source voltage, at constant drain-source voltage.

$$g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} \text{ mho or siemen.}$$

(iii) The amplification factor is defined as the ratio of the change in drain voltage to the corresponding decrease in gate voltage, at constant drain current.

$$\mu = -\left(\frac{\partial V_{DS}}{\partial V_{GS}}\right)_{I_D}$$

The minus sign indicates that when the drain voltage is increased, the gate voltage has to be decreased in order to maintain the drain current constant.

Relation connecting the FET parameters

The drain current I_D depends on the drain voltage V_{DS} and the gate voltage V_{GS},

$$I_D = f(V_{DS}, V_{GS})$$

$$\therefore dI_D = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} . dV_{DS} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}} . dV_{GS}$$

Dividing both sides by dV_{GS},

$$\frac{dI_D}{dV_{GS}} = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \cdot \frac{dV_{DS}}{dV_{GS}} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

If I_D is constant, then $\frac{dI_D}{dV_{GS}} = 0$

$$\therefore \quad 0 = \left(\frac{\partial I_D}{\partial V_{DS}}\right)_{V_{GS}} \cdot \frac{dV_{DS}}{dV_{GS}} + \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$$

$$0 = \frac{1}{r_d} \cdot (-\mu) + g_m \qquad \text{(by definition)}$$

$$\frac{\mu}{r_d} = g_m,$$

$$\therefore \mu = g_m \cdot r_d$$

$\therefore$ Amplification factor = transconductance × drain resistance.

Experiment to draw JFET characteristics (in the common source configuration) and to determine the FET parameters (JFET as an amplifier)

Connections are given with a *n*-channel JFET as shown in the fig. D.C. voltages to the drain and to the gate with respect to the source are given with the help of the potentiometers (Rh).

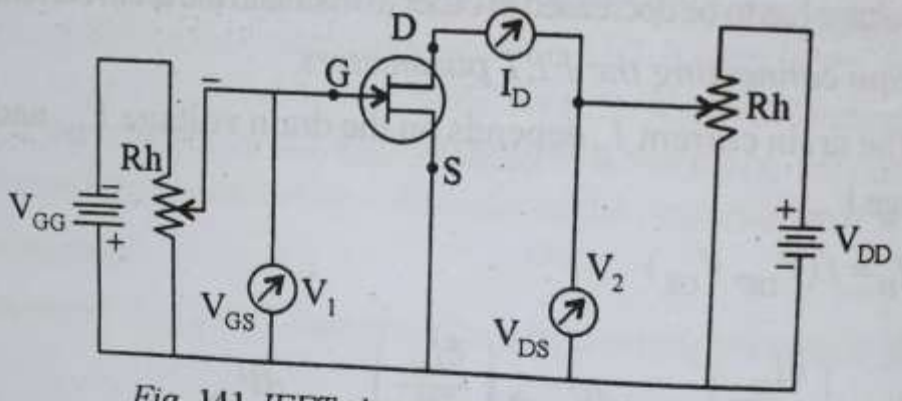


Fig. 141 *JFET characteristics study circuit.*

(i) The output or drain characteristics

Keeping $V_{GS} = 0$, the drain voltage V_{DS} is kept at 1 volt. The corresponding drain current I_D is noted. Similar I_D reading are taken for V_{DS} = 2, 3, 4 V etc upto 20V. The experiment is repeated for V_{GS} = − 0·5V, −1V, −1.5 V and −2 V. Taking the value of V_{DS} along the x-axis and the corresponding values of I_D along y-axis, a family of curves is drawn. This family of curves gives the output or drain characteristics of the JFET.

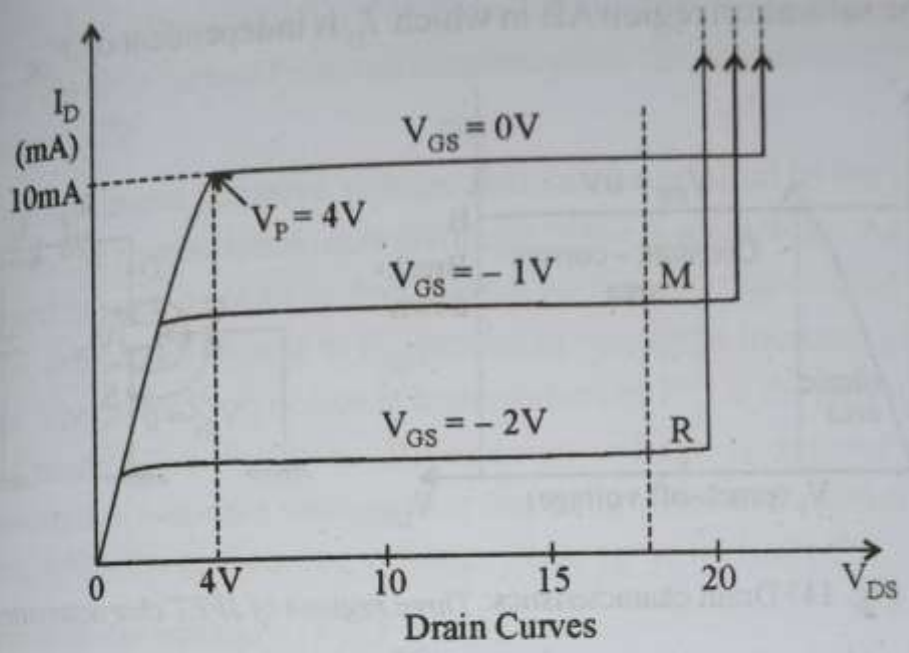


Fig. 142 *Output characteristics of JFET.*

As the voltage V_{DS} is increased, the drain current increases rapidly first and then remains almost constant (saturated). The voltage V_{DS} at which the drain-current saturates is known as *pinch-off voltage*, V_p. For $V_{GS} = 0$ volt, the value of V_{DS} at which I_D starts to level off and becomes constant is called the pinch-off-voltage, V_P. The graph (fig. 137) exhibits three regions.

(i) the ohmic region or linear region OA, where V_{DS} is small.

Here $I_D \propto V_{DS}$.

(ii) the saturation region AB in which I_D is independent of V_{DS}

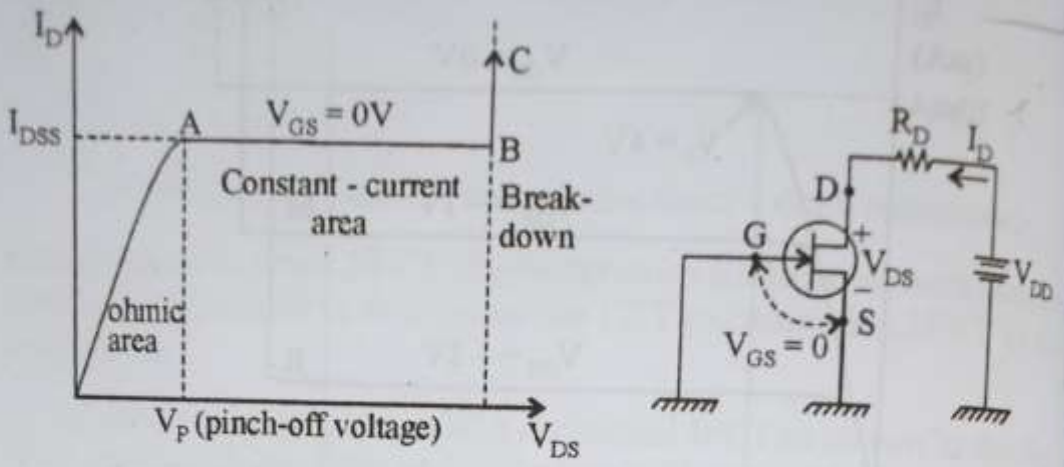


Fig. 143 Drain characteristics: *Three regions of JFET characteristics.*

(iii) the breakdown region BC where the drain current increases more or less vertically for a slight increase of V_{DS}.

To understand the nature of these curves, consider the case when $V_{GS} = 0$. When the voltage V_{DS} is increased from zero to a small amount, the *n*-channel bar acts as a simple resistor. Hence the current I_D increases linearly with V_{DS} in this region.

As the current I_D increases, the ohmic voltage drop along the bar (from the source) reverse biases the gate-source junction. This, in turn, decreases the effective channel cross-section for current conduction in the bar. Therefore, with increases in V_{DS}, the curve bends at A and finally at a value V_P of the voltage V_{DS}, the current I_D saturates. This value of drain current is I_{DSS} (drain to source current with gate shorted). I_{DSS} is the maximum drain current that a specific JFET can produce and it is always specified for the condition $V_{GS} = 0V$. The channel is now said to be pinched-off. The voltage V_P is called the pinch-off voltage. The excess voltage above V_P only broadens the depletion region and the channel is no longer affected.

(ii) the saturation region AB in which I_D is independent of V_{DS}

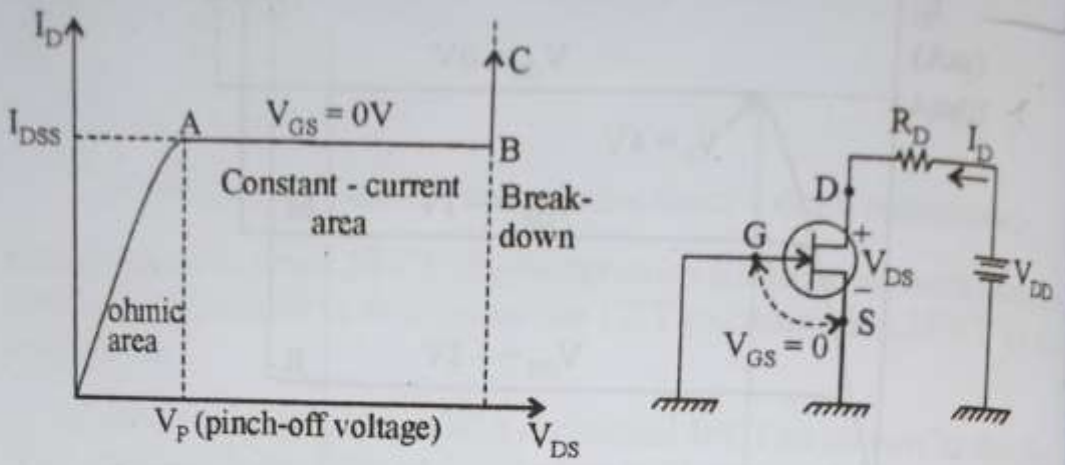


Fig. 143 Drain characteristics: *Three regions of JFET characteristics.*

(iii) the breakdown region BC where the drain current increases more or less vertically for a slight increase of V_{DS}.

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Pinch-off voltage is defined as the minimum drain-source voltage, at which the drain current becomes constant when the gate-source voltage is kept zero.

The maximum negative voltage that can be applied to the gate is limited by the reverse break-down voltage of the p-n junction. As V_{DS} is increased beyond *avalanche breakdown* voltage corresponding to the point-B, even small change in V_{DS} produces very large increase of drain current. The breakdown occurs at lesser values of V_{DS}, if the gate voltage V_{GS} is made more negative. Breakdown voltage is defined as the maximum drain-source voltage that can be applied at constant drain current, when the gate source voltage is zero (gate is shorted).

Breakdown voltage = $(V_{DS})_{max}$

In the region between pinch-off voltage (V_p) and breakdown voltage $(V_{DS})_{max}$, we see that I_{DSS} = constant. This makes the FET act as constant current source in this region. The slope of the drain curve at the saturation region for a given V_{GS} (example $V_{GS} = 0$) is found out as m.

ie., $m = \dfrac{\partial I_D}{\partial V_{DS}}$

By definition,

the drain resistance $r_d = \dfrac{\partial V_{DS}}{\partial I_D}$

Hence $r_d = \dfrac{1}{m}$ can be found out.

To find the transconductance g_m of the JFET, a vertical line is drawn corresponding to a particular value of V_{DS} (fig.). This intersects the drain curves at M and R, differing in their I_D values. Let $(V_{GS})_1$ and $(V_{GS})_2$ be the values at M and R, differing in their V_{GS} values. The corresponding drain current values are noted from the graph as $(I_D)_1$ and $(I_D)_2$.

The transconductance $g_m = \left(\frac{\partial I_D}{\partial V_{GS}}\right)_{V_{DS}}$ by definition.

$$\therefore g_m = \frac{(I_D)_1 - (I_D)_2}{(V_{GS})_1 - (V_{GS})_2}$$

Knowing r_d and g_m, the amplification factor μ of the FET can be calculated using the relation:

$$\mu = r_d \times g_m$$

(ii) *The transfer characteristics : Cut - off voltage*

The transfer characteristics relates the output drain current to the input gate voltage. The drain-source voltage V_{DS} is kept fixed at a constant value, say 15V. Keeping $V_{GS} = -1$V, the drain current I_D is noted. Similar readings are taken for I_D with $V_{GS} = -2, -3, -4$V. Taking V_{GS} along the negative x-axis and I_D along y-axis, a graph is drawn (fig.). This gives the transfer characteristics of the FET. The graph is a non-linear curve.

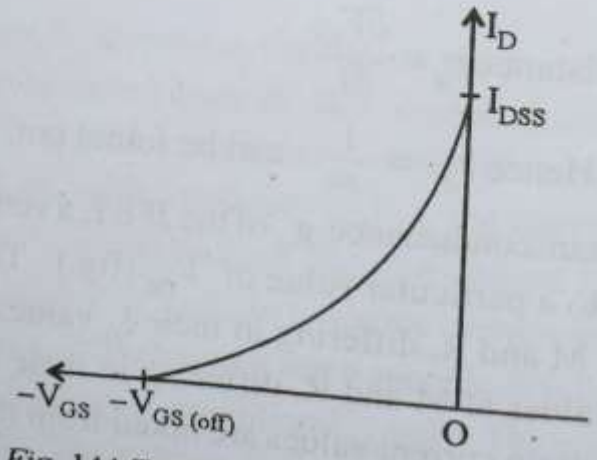


Fig. 144 Transfer characteristics of JFET.

For constant V_{DS}, as the reverse voltage ($-V_{GS}$) is increased, the drain current I_D decreases. The value of V_{GS} which makes $I_D = 0$ is known as the cut-off voltage $V_{GS(off)}$. For JFET, the pinch-off voltage

$$V_P = -V_{GS(off)}.$$

The JFET must be operated at any point in the transfer characteristics curve between I_{DSS} and $V_{GS(off)}$. The equation to the curve is

$$I_D = I_{DSS} \times \left(1 - \frac{V_{GS}}{V_{GS(off)}}\right)^2$$

This is an empirical formula for drain current.

When $V_{GS} = 0$, there is maximum current flowing through the channel as the depletion layer width is now the smallest and channel is wider. The maximum current is termed I_{DSS}.

The position of the pinch off voltage (at which the drain current I_D levels off) in the transfer characteristics ($V_{DS} - I_D$ curve) for $V_{GS} = 0$ is shown as V_P.

Obviously, $V_P = -V_{GS(off)}$

$$V_P = |V_{GS(off)}|$$

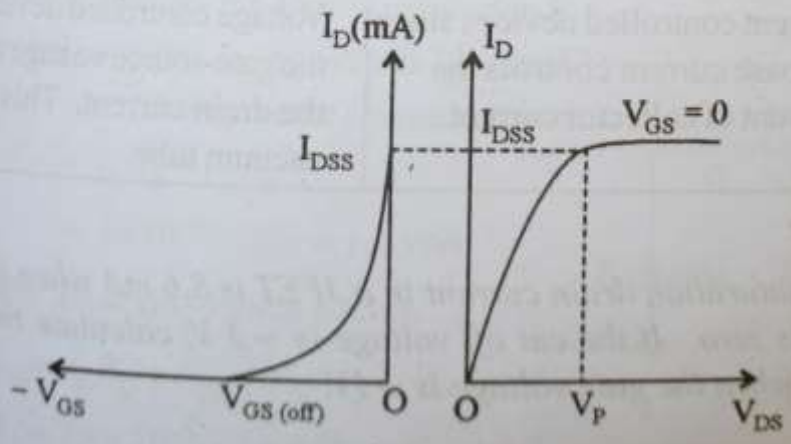


Fig. 145 $-V_{GS(off)} = V_P$

Comparison between n-channel JFET and p-channel JFET

	n - channel JFET	p - channel JFET
1.	The current carriers are electrons	holes
2.	Mobility of electrons large	poor
3.	Trans conductance g_m large	small
4.	Input noise low	large

Comparison between junction transistor (BJT) and JFET
(Importance of JFET)

	Bipolar Junction Transistor (BJT)	Junction Field Effect Transistor (JFET)
1.	Input resistance : low	very high
2.	Transconductance : very high	low
3.	More noisy	less noisy
4.	Thermal stability : poor	good
5.	Less costly	more costly
6.	Sensitive to radiations	immune to radiations
7.	Bipolar device	Unipolar device
8.	Current controlled device : since the base current controls the amount of collector current.	Voltage controlled device:since the gate-source voltage controls the drain current. This is like vacuum tube.

Example

Questions

1. Explain transistor action and show how base current is produced. Define transistor α and transistor β and prove that $\left(\frac{1}{\alpha} - \frac{1}{\beta}\right) = 1$.
2. Describe, giving circuit diagrams, the three modes of transistor connection. Compare the performances of the three modes of transistor connection and find the relation connecting transistor α, β and γ parameters.
3. Explain Q point, load line and stablisation of transistor, functioning as amplifier. Define stability factor. Mention its significance. Derive an expression for stability factor, analysing a transistor in CE mode with fixed bias.
4. Giving relevant circuit diagram, excplain the function of various components in a paractical transistor CE amplifier. Derive an expression for voltage gain and power gain of the amplifier.
5. Draw the circuit diagram of a practical transistor CE amplifier of R.C. coupled type and explain its working. Deduce the voltage gain of the amplifier in terms of its input impedance.
6. Draw the circuit diagram of transformer coupled amplifier and explain its working. Find an exprssion for over all gain. What are its advantages and disadvantages ?.
7. What is meant by biasing a transistor? What is the need for biasing? Explain, with necessary circuit diagrams the methods of (i) base resistor bias (ii) collector feed back resistor bias and (iii) voltage divider bias. Which one is superior? Justify your answer.
8. Explain, with circuit diagram, the method of potential divider bias. Obtain the coordinates (V_{CE}, I_C) of the operating point. What are the advantages of using this method of biasing?
9. Discuss the relative advantages of the three common methods of biasing transistor amplifier.

10. Draw the circuit diagram of a simple power amplifier with transistor and explain its action. Obtain expression for its collector efficiency.
11. Draw the block diagram of a power amplifier. Bring out the differences between voltage amplifier and power amplifier. Why are power transistors bigger in size and provided with heat sink?
12. Explain how power amplifiers are classified. Compare the performance of various classes of power amplifier.
13. Draw the circuit diagram of a push-pull transistor power amplifier and explain its functioning. What is the requirement on coil winding in the output transformer for maximum power output?
14. Describe the structure of JFET and explain its working principle. Bring out the difference between JFET and bipolar junction transistor. Write about the importance and advantages of FET.
15. Explain the action of JFET as an amplifier.
16. Define JFET parameters. Obtain the relation connecting them. Draw the output characteristics of a JFET and show how the JFET parameters could be determined from it. Give an expression for drain current.

Objective type questions

1. Which is the largest current in a p-n-p transistor functioning in an amplifier circuit?

(a) emitter current (b) base current

(c) collector current (d) output current

2. Push pull amplifier is operated mostly under

(a) class A (b) class B

(c) class C (d) class D condition

3. When the by-pass capacitor in the emitter circuit of a CE trasistor amplifier (or JFET amplifier) is removed, the gain of the amplifier.

(a) remains unaffected (b) is decreased

(c) is increased (d) non of the above

4. The figure of merit or transconductance (g_m) of a transistor is the ratio

(a) $\left(\frac{h_{fe}}{h_{ie}}\right)$ (b) $\left(\frac{h_{ie}}{h_{oe}}\right)$ (c) $\left(\frac{h_{re}}{h_{fe}}\right)$ (d) $\left(\frac{h_{re}}{h_{ie}}\right)$

5. The slope of d.c. load line for an amplifier is equal to

(a) R_C (b) $-R_C$ (c) $1/R_C$ (d) $-1/R_C$

6. The efficiency of a power amplifier is the ratio of the power delivered to the load to

(a) the input signal power

(b) power dissipated in the last stage

(c) power from the d.c. power supply

(d) the voltage across the load

7. The power amplifier in which current flows for only one half cycle of the input signal is classified as

(a) class A (b) class B (c) class C (d) class AB

8. For clalss-A amplifier, Q-point on the d.c. load line is at

(a) middle (b) one - end

(c) the other end (d) the origin

9. The phase difference between output and input of CE transistor amplifier is

(a) 2π (b) π (c) zero (d) $\pi/2$

10. Supply voltage to collector is +10V. At cut off condition, the d.c. voltage at the collector is

(a) 20V (b) 5 V (c) 2V (d) 10V

11. In a CE transistor amplifier, voltage gain is

(a) $\alpha \frac{R}{R_L}$ b) $\beta \frac{R}{R_L}$ c) $(1+\alpha) \frac{R}{R_L}$ d) $(1+\beta) \frac{R}{R_L}$

12. If R_C and R_L are the collector resistance and load resistance respectively in a single stage transistor CE amplifier, the a.c. load is

(a) $(R_L + R_C)$ (b) $(R_L - R_C)$ (c) $R_C \| R_L$ (d) R_C

13. In a single stage transistor CE amplifier, if Rc and R_L are the collector resistance and load resistance respectively, the transistor sees a d.c. load of

(a) R_L (b) R_C (c) $(R_C + R_L)$ (d) $R_C \| R_L$

14. Large value of stability factor means

(a) good stability of Q - point (b) poor stability of Q - point

(c) medium stability of Q - point (d) none of the above

15. Common collector circuits are mostly used for

(a) high voltage gain (b) low voltage gain

(c) impedance matching (d) all the above

16. In a transistor amplifier, stabilisation is achieved due to the action of

(a) R_E (b) R_C (c) R_L (d) $R_C \| R_L$

17. Q - point is independent of β of transistor in

(a) base resistor bias b) collector feed back resistor bias

(c) voltage divider bias d) emitter feed back resistor bias

18. Class C power amplifier has its Q - point fixed at

(a) midpoint of ' ad line (b) above cut-off voltage

(c) below cut-o (d) at cut - off voltage

19. A JFET is a

(a) voltage controlled device (b) current controlled device

(c) low input resistance device (d) constant current source

20. The input impedance of JFET is

(a) zero (b) one (c) very large (d) very small

21. The pinch-off voltage in a JFET has the same magnitude as

(a) the gate voltage (b) drain - source voltage

(c) gate-source voltage (d) gate-source cut off voltage

22. When the gate voltage becomes more negative in a *n*-channel JFET, channel width

(a) decreases (b) increases

(c) diappears (d) is not affected

23. The input current of JFET is

(a) a few microamperes (b) negligibly small

(c) a few milliamperes (d) a few amperes

24. In a JFET, I_D is maximum where V_{GS} is

(a) zero (b) negative (b) positive (d) equal to V_P

25. The JFET is a

(a) unipolar device (b) voltage-controlled device

(c) current -controlled device (d) answers (a) and (b)

26. The constant current area of a JFET lies between

(a) cut-off and saturation (b) cut-off and pinch-off

(c) zero and I_{DSS} (d) pinch-off and break-down.

27. Siemen is the unit for

(a) impedance (b) conductance

(c) transconductance (d) magnetic flux

28. The input control parameter of JFET is

(a) gate voltage (b) source voltage

(c) drain current (d) gate current

29. In a JFET, I_{DSS} stands for

(a) drain to source current

(b) drain to source current with gate shorted

(c) drain to source current with gate open

(d) none of the above

30. Which of the following device has the highest input impedance?

(a) JFET (b) BJT

(c) crystal diode (d) none

31. FET is

(a) a unipolar device (b) bipolar device

(c) unijunction device (d) all the above

32. When JFET is cut off, the depletion layers are

(a) far apart (b) close together

(c) touching (d) conducting

33. When the gate voltage becomes more negative in *n*-channel FET, the channel between the depletion layers

(a) shrinks (b) expands

(c) conducts (d) stops sonducting

34. A JFET has $I_{DSS} = 8$ mA and $V_p = 4$V. Their r_{DS} is

(a) 200 ohm (b) 320 ohm (c) 500 ohm (d) 5 k ohm

35. The expression for drain current in a FET is

(a) $I_D = I_{DSS} \times \left(1 + \frac{V_{GS}}{V_{GSoff}}\right)^2$ (b) $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_{GSoff}}\right)^2$

(c) $I_D = I_{DSS} \times \left(1 + \frac{V_{GS}}{V_{GSoff}}\right)$ (d) $I_D = I_{DSS} \times \left(1 - \frac{V_{GS}}{V_{GSoff}}\right)$

36. When the gate voltage of a FET is half the cut off voltage, the drain current is _____ of the maximum

(a) one half (b) one third

(c) one fourth (d) one eighth

37. In a FET the gate controls

(a) width of the channel (b) the drain current

(c) the gate voltage (d) all the above

38. The gate of a JFET is _____ biased

(a) forward (b) reverse

(c) both reverse and forward (d) none of the above

39. The input control parameter of a JFET is

(a) source voltage (b) drain voltage

(c) gate current (d) gate voltage

40. The two important advantages of JFET are

(a) low input impedance and high output impedance

(b) in expensive and high output impedance

(c) high input impedance and square law property

(d) none of the above

41. In a C.E. amplifier the presence of by -pass capacitor

(a) increases the voltage gain (b) decreases the voltage gain

(c) increases the impedance (d) all the above.

Answers

1 (a)	1. (b)	3. (b)	4. (a)	5. (d)
6 (c)	7. (b)	8. (a)	9. (b)	10. (d)
11 (b)	12. (c)	13. (b)	14. (b)	15. (c)
16. (a)	17. (c)	18. (d)	19 (a)	20 (c)
21 (d)	22 (a)	23 (b)	24 (c)	25 (d)
26(d)	27 (c)	28 (a)	29 (b)	30 (a)
31 (a)	32 (c)	33 (a)	34 (c)	35 (b)
36 (c)	37 (d)	38 (b)	39 (d)	40 (c)
41 (a)				

UNIT-IV

OSCILLATORS AND WAVE SHAPING CIRCUITS

Feedback principle and Barkhaussen criterion - Hartley , Colpitt's, and Phase shift oscillators using transistors – Astable - Monostable and Bistable multi vibrators using transistors - Schmitt trigger - clipping and clamping circuits - Differentiating circuit - Integrating circuit.

Feedback principle

In an amplifier, a small part of the output signal may be fed to the input circuit by suitable means. This is known as feed back. When the feedback voltage is in phase with the input signal voltage, the feedback is said to be positive or regenerative feedback. If the feedback voltage is opposite in phase to the input signal, it is said to be negative or degenerative feedback. Thus, there are two types of feedback: (1) positive feedback and (2) negative feedback.

The positive feedback is used in oscillators and the negative feedback in amplifiers.

The voltage feedback may be proportional to the output voltage across the load or it may be proportional to the current through the load. In the former case, the feedback is voltage feedback and in the latter case it is current feedback.

The amount of feedback is determined by the feedback network. The circuit can also vary the feedback amount for different frequencies. The amount of amplifier gain with feedback is called the *closed loop gain*. Without feedback, the gain is called *open loop gain*.

1. *The effect of feed-back on the gain of an amplifier*

Let A be the gain of an amplifier without feedback. If v_o and v_i be the output and input voltages respectively, then the open loop gain is given by

$$A = \frac{v_o}{v_i} \qquad \ldots\ \ldots\ \ldots\ (1)$$

A fraction β of the output v_o is feedback into the input circuit through the feedback circuit. Let the feedback ratio be β. This is,

$$\beta = \frac{v_f}{v_o}.$$

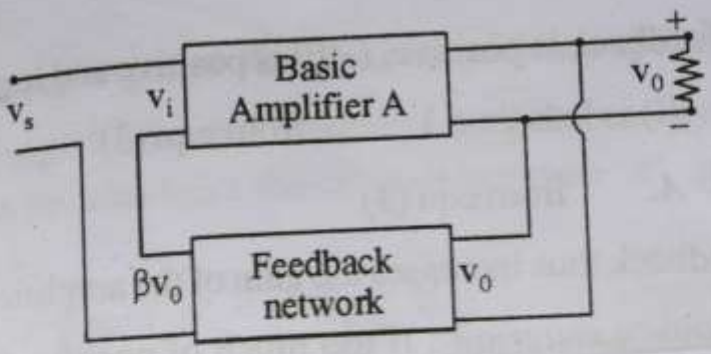


Fig.147 Effect of feed back on gain of amplifier.

Then the voltage feedback is $v_f = \beta v_o$.

If v_s is the voltage supplied by the source to the amplifier, the total input voltage is

$$v_i = v_s + \beta v_o \quad \text{(since the } \beta v_o \text{ is in phase with } v_s\text{)} \quad \ldots\ldots\ldots (2)$$

From equation (1), $v_o = A\, v_i$

Substituting the value of v_i from equation (2)

$$v_o = A\,(v_s + \beta v_o)$$

$$v_o = A v_s + A\beta v_o$$

$$\therefore\ v_o(1 - A\beta) = A v_s$$

$$\therefore\ \frac{v_o}{v_s} = \frac{A}{(1 - A\beta)}$$

The ratio (v_o / v_s) gives the closed loop gain of the amplifier A' with feedback. ie, $A' = v_o / v_s$

$$\therefore\ A' = \frac{A}{(1 - A\beta)} \quad \ldots\ldots\ldots (3)$$

Discussion : *Negative and Positive feedback*

Case 1 : If the feedback is negative, $A\beta$ is negative. (either A or β negative).

Then, $A' = \dfrac{A}{(1 + A\beta)}$ from eqn .... (3)

$\therefore\ A' < A.$

The negative feedback thus decreases the gain of the amplifier.

Case 2 : If the feedback is positive, ($A\beta$) is positive and less than 1,

$\therefore$ $(1 - A\beta)$ is less than 1. ..... from eqn (3)

$\therefore$ $A' > A$. from eqn (3)

The positive feedback thus increases the gain of the amplifier.

Case 3 : *Barkhausen criterion* : If too much of positive feedback is given such that $A\beta = 1$, then $1 - A\beta = 0$.

$$\therefore \quad A' = \frac{A}{0} = \infty$$

If $|A\beta| = 1$, the gain $A' = v_o / v_s$ becomes infinite. ie., there is output without any external input signal. However, the output is not constant but varies with time, the rate of variation depending on the circuit parameters. The amplifier circuit under this condition becomes unstable and has a tendency to oscillate. It generates electrical oscillations at the output and it is said to behave as an oscillator. Thus, the condition under which an amplifier works as an oscillator is

$$|A\beta| = 1 \qquad ie., \quad A = \frac{1}{|\beta|}$$

As β is a fraction, the gain of the amplifier should be greater than unity.

The amplifier produces a phase difference of 180° between the input and the output signals. If the feedback circuit further produces 180° phase difference, the net effect (180 + 180 = 360) will be that the feedback signal is in phase (360° = 0°) with the signal at the input side. This kind of feedback is known as positive regenerative feedback and it helps oscillation to build up.

Thus, *the conditions for sustained oscillations are*

1. The feedback factor $|A\beta| = 1$, and
2. the net phase shift around the loop = integral multiple of 2π (or 360°) ie., the feedback must be positive.

The above requirement is called *Barkhausen criterion for oscillation*.

2. *Effect of negative feedback on stability of the amplifier*

The negative feedback reduces the gain but improves the stability. This can be seen from the relation between A' and A for negative feedback.

Closed loop gain $A' = \frac{A}{1 - A\beta}$. If β is very large, the quantity $A\beta > 1$.

Then, $A' = \frac{A}{A\beta}$

$\therefore \quad A' = \frac{1}{\beta}$

The term β is the feedback ratio and it is a function of the feedback network only. It does not depend upon the amplifier parameter changes or supply voltage variations. So, the gain is steady. Thus the negative feedback improves stability of gain of the amplifier.

Advantages of negative feedback

1. Negative feedback stabilises an amplifier. The gain becomes independent of the transistor parameters and temperature.
2. Negative feedback increases the input impedance of an amplifier, which will not then draw much current from the source.
3. Negative feedback decreases the output impedance of an amplifier, which can then supply large amount of current to the load (speaker).
4. The output noises and hum in an amplifier can be reduced by negative feedback.
5. The distortion in the output is reduced, because there is partial cancellation of out-of-phase signals. Both amplitude distortion and frequency distortion are reduced.
6. The negative feedback increases the bandwidth of an amplifier, but decreases its gain.

Functions of the tank circuit in oscillators

1. The tank circuit is an essential part of an oscillator. It provides feedback path so that part of output is feedback to the input.
2. The tank circuit produces a phase shift of 180° (or π) between the output and input from the tank.
3. The tank circuit produces attenuation in the signal feedback so that only a portion of the output of the amplifier is fedback.
4. The tank circuit decides the frequency of oscillation in the oscillator. The frequency depends on the tank circuit parameters such as L and C.

Oscillators

An oscillator is an amplifier with sufficient gain and positive feedback. It produces a periodically varying voltage waveform at its output v_o, even without any external input. The oscillator actually draws electric energy for this purpose from the d.c. power supply connected to the oscillator.

Essential parts of an oscillator

An oscillator has essentially the following sections:

1. An amplifier with external regenerative feed back to provide a negative resistance in the circuit.
2. Some nonlinear circuit element (like transistor) to fix the amplitude of oscillation.
3. A net-work to produce oscillation at the desired frequency. This part is known as the tank circuit.
4. A.d.c. power supply.

Starting voltage in an ascillator

Every resistor contains some free electrons. At the room temperature, these free electons move randomly in different directions and generate a noise voltage across the resistor. This voltage may be of a large range of frequencies, ie., each resistor is a small a.c. voltage source producing all frequencies.

When we first switch on the power supply of the oscillator, the only signals in the system are the noise voltages generated by the resistors. These noise voltages are amplified and appear at the output terminals. The amplified noise passes through the feed back circuit and appear at the inputs in phase. Thus the oscillator starts functioning.

Colpitt's oscillator

One basic type of resonant circuit feedback oscillator is the Colpitt's oscillator. The Colpitt's oscillator generates sinusoidal output waves.

Circuit diagram

A Colpitt's oscillator using an *npn* transistor in the common emitter mode is shown in the diagram. It is an amplifier with positive feedback arrangement. The transistor amplifier contains R_C as the load resistance, and R_E as the emitter resistance and C_E the by-pass capacitor to provide the *a.c.* path. V_{CC} is the power supply to the transistor. The resistors R_1 and R_2 form the potential divider. The

voltage across R_2 gives the necessary base bias to the transistor. The input to the amplifier appears to the base through the capacitor C. The output is available at the collector through the capacitor C with respect to the ground.

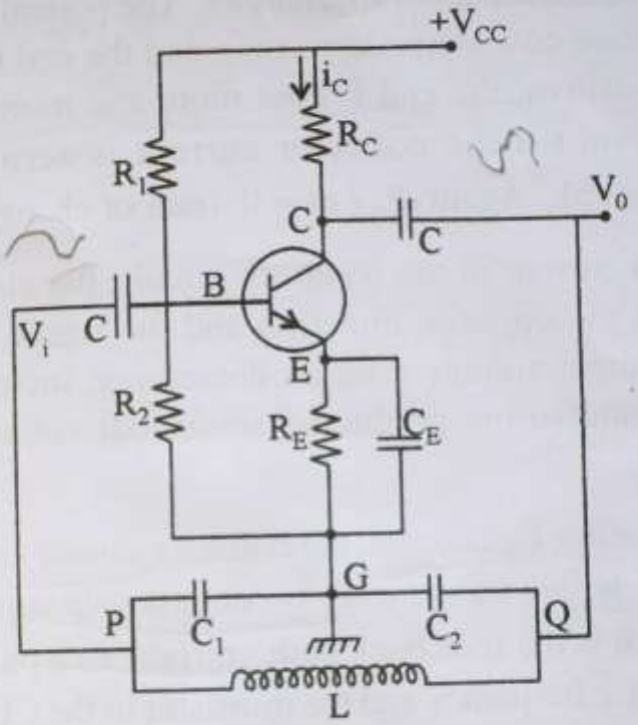


Fig. 154 *Colpitts oscillator.*

The value of the components R_E and R_C are chosen such that the gain of the amplifier is greater than unity ($A > 1$).

The feedback circuit is a tank circuit containing inductance L and capacitance C_1 and C_2 as shown. Because of the earth connection at G, the potentials at Q and P are 180° out of phase. If Q is positive-going, P will be negative - going in potential.

Working

When the switch is closed, the collector current starts increasing. The potential at the collector V_C starts decreasing, making the end Q negative - going in potential. Hence the potential at P is positive going. This makes the transistor to conduct more and more due to positive feedback action. The collector voltage continues to decrease

till $V_C = 0$, ie., the transistor is in saturation conducting the maximum current. Now, the rate of current variation $(dI_C / dt) = 0$.

With no current in the feedback path, the electric field in C_1 collapses and the capacitor discharges. The potential at P and hence that at the base now starts decreasing and the end Q becomes more and more positive; the end P goes more and more negative. This

trend goes on till the collector current is zero and $V_C = V_{CC}$ (the maximum). Again $dI_C / dt = 0$. (rate of change)

With no current in the feedback circuit, the electric field in C_1 collapses in the opposite direction and the whole process repeats. Thus, the output voltage goes on decreasing, increasing and again decreasing and so on, producing sinusoidal voltage waves at the output.

The capacitor C_2 couples, the collector circuit energy back to the tank circuit. In this way, energy is continuously supplied to the tank circuit, which is the feed back path, introduces a phase shift of 180° at its resonance frequency and the transistor in the CE mode produces a phase shift of another 180° between the input and the output. Thus the net phase shift around the loop = 2π radian and there is strong positive feedback. As these two conditions are satisfied, the circuit readily functions as an oscillator and the electrical oscillators are maintained. The LC tank circuit provides the necessary phase shift and acts as a resonant filter that passes only the desired frequency of oscillation.

The frequency of oscillation is given by

$f = \frac{1}{2\pi\sqrt{LC}}$ where $\frac{1}{C} = \frac{1}{C_1} + \frac{1}{C_2}$ and L is the inductance of the coil in the tank circuit.

Sustained oscillations are produced if $h_{fe} \geq \frac{C_1}{C_2}$ where h_{fe} is the forward current gain of the transistor used.

The oscillator can be set into working by adjusting the value of C_1 and C_2 initially. The frequency of oscillation can be changed by gang - tuning the two capacitors C_1 and C_2.

Colpitt's oscillator can be used to produce electrical oscillations of a wide range of frequencies from 1 to 500 MHz. Colpitt's oscillator is widely used in commercial signal generations above 1 mega hertz frequency.

Condition for oscillation

For an oscillator to start functioning, the positive feedback must be strong, ie., $A\beta > 1$.

where A is the open loop gain and β is the feedback ratio.

For the common emitter amplifier circuit used in the oscillator, the voltage gain $A = \frac{R_C}{r_e}$ where R_C is the load resistance and r_e is the dynamic resistance of the base-emitter junction.

$$\therefore A = \frac{R_C}{r_e} > \frac{1}{\beta} \quad \ldots\ldots\ldots (1)$$

Now, the feedback ratio $\beta = \frac{\text{voltage feed to base}}{\text{output voltage at the collector}} = \frac{V_f}{V_o}$

Hartley Oscillator

Hartley osciallator is a type of oscillator circuit which generates sinusoidal output signals i.e., the output voltage varies with time as a sine curve.

Hartley oscillator circuit using *npn* transistor in the common emitter mode, is shown in the diagram. It is an amplifier with a positive feed back arrangement. The transistor amplifier contains R_C as the load resistance, R_E as the emitter resistance and C_E the by-pass capacitor to provide the a.c. path. V_{CC} is the power supply to the transistor. The resistance R_1 and R_2 form the potential divider arrangement. The voltage across R_2 gives the necessary base bias to the transistor. The input to the amplifier appears to the base through the capacitor C_1. The output is available at the collector through the capacitor C_2 with respect to the ground. The value of the components R_C and R_E are chosen such that the stage gain of the amplifier is greater than unity ($A > 1$).

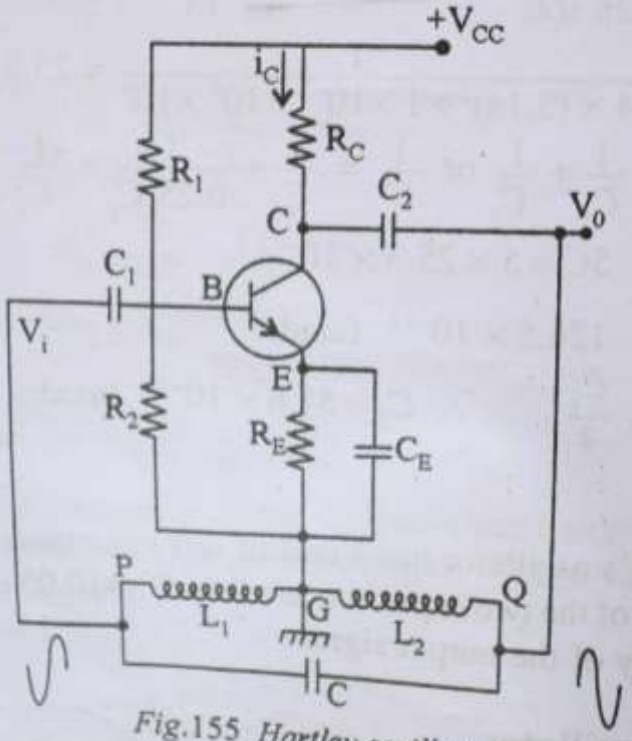


Fig.155 *Hartley oscillator*

The feedback circuit is a tank circuit containing inductances L_1 and L_2 and a variable capacitance C. L_1 and L_2 are inductively coupled i.e., any change of flux in L_1 occurs at L_2 also.

Because of earth connections at G, the potential at Q and P are 180° out of phase. If Q is positive going, P will be negative going in potential.

Working

When the switch S is closed, the collector current starts increasing. The potential at the collector V_C starts decreasing, making the end Q negative going in potential. Hence the potential at P is positive going. This makes the transistor to conduct more and more due to positive feed back action. The collector voltage continues to decrease till $V_C = 0$ i.e., the transistor is in saturation, conducting the maximum current. Now rate of change of collector current $\frac{dI_C}{dt} = 0$.

With no current in the feedback path, the magnetic field in L_1 collapses and discharges the capacitor. The potential at P and hence that at the base now starts decreasing and the collector current starts decreasing. This causes V_C to increase and the end Q becomes more and more positive and the end P goes more and more negative. This trend goes on till the collector current is zero and $V_C = V_{CC}$ (the maximum). The transistor is now in cut-off state.

Again $\frac{d I_C}{dt} = 0$.

With no current in the feedback circuit, the magnetic field in L_1 collapes in the opposite direction and the whole process repeats. Thus the output voltage goes on decreasing, increasing and again decreasing and so on, producing sinusoidal voltage waves at the output.

The coil L_2 couples the collector circuit energy back to the tank circuit by means of the mutual inductance between L_1 and L_2. In this way energy is continuously supplied to the tank circuit to overcome the energy losses in the tank circuit. The LC tank circuit, which is the feedback path, introduces a phase shift of 180° (π radian) at its resonant frequency and the transistor in the common emitter mode produces a phase shift of another 180° (π radian) between input and the output. Thus, the net phase shift around the loop = 2π

radian, and there is strong positive feedback. As these two conditions are met with, the circuit readily functions as an oscillator and the elelctrical oscillations are maintained.

The frequency of oscillations is given by

$$f = \frac{1}{2\pi\sqrt{LC}}$$

when $L = L_1 + L_2 + 2M$. Here M denotes mutual inductance between the two coils of self inductance L_1 and L_2. C is the capacitance in the tank circuit. Sustained oscillations will be produced if

$$h_{fe} \geq \frac{L_2 + M}{L_1 + M}$$

where h_{fe} is the forward current gain of the transistor. The oscillator can be set into working by adjusting the value of L_1 or L_2 initially.

The frequency of oscillations can be changed by varying the capacity of the capacitor C in the tank circuit. The Hartley oscillaor is easy to tune. It can be used to produce electrical oscillations of a wide range of frequencies. Hartley oscillator is commonly used as high frequency local oscillator in radio receivers and for production of ultrasonic waves using piezo-electric crystal in the tank circuit.

Condition for oscillation

For an oscillator to start functioning, the positive feed back must be strong. ie., $A\beta > 1$;

$\therefore A > \frac{1}{\beta}$ where A is the open loop gain and β is the feed back ratio.

For a common emitter amplifier circuit used in this oscillator, the

voltage gain $A = \frac{R_C}{r_e}$.

where R_C is the load resistance and r_e is the dynamic resistance of the base-emitter junciton. Since $A > \frac{1}{\beta}$

$$\therefore \frac{R_C}{r_e} > \frac{1}{\beta} \quad \ldots\ldots\ldots (1)$$

The feedback ratio $\beta = \frac{\text{voltage fed to the base}}{\text{output voltage at the collector}}$

$$\beta = \frac{v_f}{v_o}$$

The output voltage is across L_2 and the feed back voltage is across L_1.

$$\therefore \beta = \frac{i L_1 \omega}{i L_2 \omega}$$

where i is the circulating current at any instant in the tank cicruit.

$$\therefore \beta = \frac{L_1}{L_2}$$

Using this value in equation (1), $\frac{R_C}{r_e} > \frac{L_2}{L_1}$

In terms of h_{fe} of the transistor,. since the gain $A = h_{fe}$.

$$h_{fe} > \frac{L_2}{L_1} \qquad (\text{since } A = \frac{R_C}{r_e}).$$

This is the condition for oscillation.

Phase Shift RC oscillator

L C circuits are used to control the frequency of oscillation of Hartley and Colpitt's oscillators. It is possible to use *R C* circuits also to fix the frequency of an oscillator. This is done in a phase shift oscillator.

Principle

Consider an *R C* network, connected in series with a signal generator of angular frequency ω. Let *i* be the current at any instant through the circuit. The voltage drop across the resistor is $V_R = iR$. This is in phase with the current i. The voltage drop across the capacitor is $V_C = \frac{i}{C\omega}$. This lags behind the current by π /2 or 90°.

Taking the direction of current as the reference axis, the above two voltages are represented in a vector diagram with OM for V_R and ON for V_C. The resultant of vector OM and vector ON is vector OP. If ϕ is the phase difference between input (across AG) and the output (across BG).

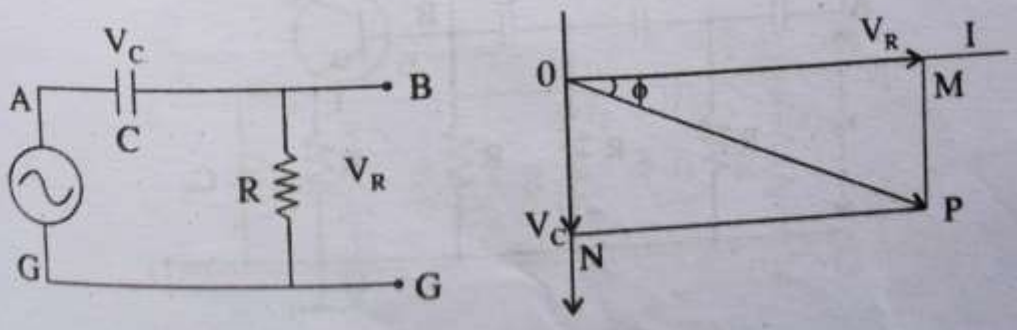


Fig. 156 R-C phase shift network

$$\tan\phi = \frac{V_C}{V_R} = \frac{i/\omega C}{iR} = \frac{1}{C\omega R}$$

For a fixed desired frequency, the value of C or R can be adjusted so as to have $\phi = 60^0$ i.e., $\tan 60 = \sqrt{3} = \frac{1}{C\omega R}$. With these values for C and R, the network is capable of producing a phase shift by 60^0.

By constsructing a ladder of three such net works in series, a total phase shift $= 3 \times 60^0 = 180^0$ can be produced between the input and the output. This network can be used as the feed back path to a CE amplifier so as to obtain a phase shift oscillator.

Circuit diagram

The circuit diagram of a phase shift oscillator, employing a CE transistor amplifier and a CR ladder network is shown in fig. R_C is a collector load resistor and R_E is the emitter resistor. The CR ladder network is connected across the base and the emitter. The ladder is the feed back path for the oscillator. The ladder is constructed for a particular frequency f.

Working

The input to the ladder is v_o; which is the oscillator output voltage signal. Let v_i be the input to the CE amplifier. This is obtained from the ladder output as shown.

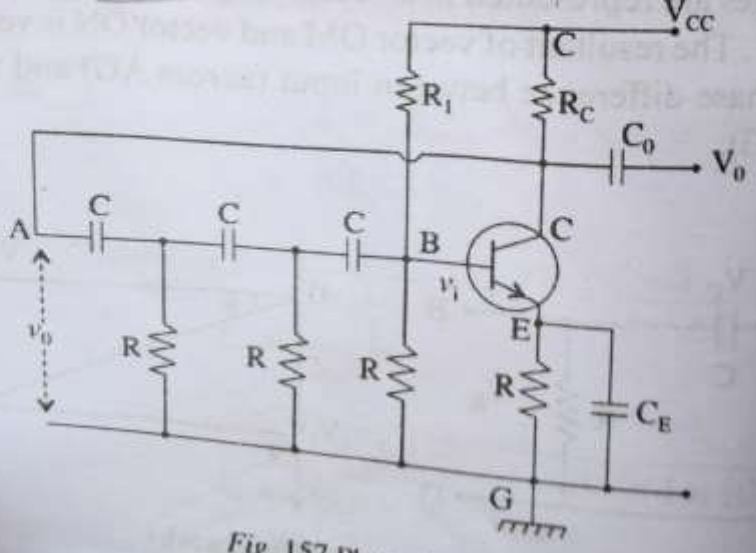


Fig. 157 Phase shift oscillator

The signal at the collector is 180^0 out of phase with the signal at the base. The ladder net work gives an additional 180^0 phase shift. So, the base receives in-phase feedback at all instants. This is because $180^0 + 180^0 = 360^0$ and 360^0 is the same as 0^0 in circular measurement. If the gain A of the amplifier is such that $A\beta$ is greater than unity at the particular frequency f, oscillations can start. The oscillator produces sine wave output voltage continuously.

The frequency of oscillation is give by $f = \dfrac{1}{2\pi RC\sqrt{6}}$

The minimum voltage gain required for oscillation is $A = -29$.

Advantages of phase shift oscillator

1. The output frequency is stable.
2. The circuit can be used for producing oscillations of even very low frequencies.
3. The circuit does not require inductors of transformers

Disadvantages of phase shift oscillator

1. This oscillator cannot be used to gererate signal of high frequencies.
2. As feedback is small, it is not easy to start oscillations.
3. The output voltage of the oscillator is small.

Multivibrators using transistors

Electronic oscillators can be classifield into two types: (1) sinusoidal oscillators and (2) Non - sinusoidal oscillators.

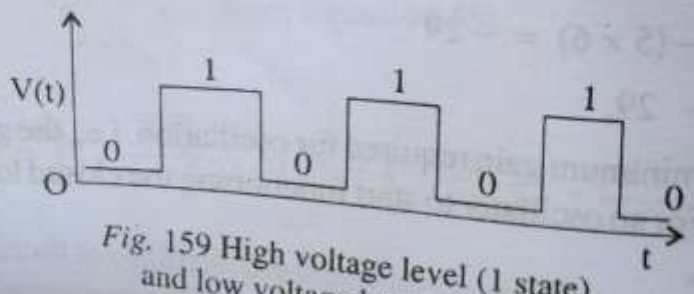


Fig. 159 High voltage level (1 state) and low voltage level (0 state)

The Hartley oscillator, Colpitt's oscillator, R-C Phase shift oscillator and Wein bridge oscillator are examples of sinusoidal oscillators since they generate output voltage varying as a sine wave.

There is a class of R- C coupled oscillators which generate nonsinusoidal waves at the output such as square wave, rectangular wave or saw-tooth wave. This class of oscillators is called *Multivibrators* (MV). Instead of generating sine waves, the Multivibrators produce oscillations between the 'high' voltage level (1 state) and the 'low' voltage-level (0 state) at the output terminal.

One cycle includes the time for a high state and a low state. When each level takes the same time, the output is a symmetrical square wave. With unequal times, the circuit produces unsymmetrical pulses. The output voltage levels oscillate between high and low levels because of the changes between the conduction and cut-off states of the device (transistor or op-amp) used in the multivibrator circuit. This type of oscillator is sometimes called a *relaxation oscillator,* because of the period of cut off. i.e., the device alternately supplies power to the load at the output and relaxes when it is in cut-off.

1. Multivibrators may be self-excited, requiring no external excitation, i.e., they may not need any input signal. In this case, neither of the two output states (high or low) is stable. Such multivibrators are known as astable multivibrators. The output levels successively change from one state to the other. For this reason, the astable multivibrators are also called free-running multivibrators.

2. Multivibrators may also be 'driven' oscillators whose working is controlled by external driving voltages. Since external driving input pulses (voltages) are required, the driven multivibrators are not strictly 'oscillators'.

There are two type of driven multivibrators :

(a) the monostable multivibrators (one-shot MV) and

(b) the bi- stable multivibrators (flip-flops).

1. Astable multivibrator (free-running multivibrator)

The Astable multivibrator has two quasi-stable states. It switches back and forth from one state to the other, remaining in each state for an interval of time, depending upon the discharging of a CR-circuit. Thus it is an oscillatory circuit and it requires no external triggering.

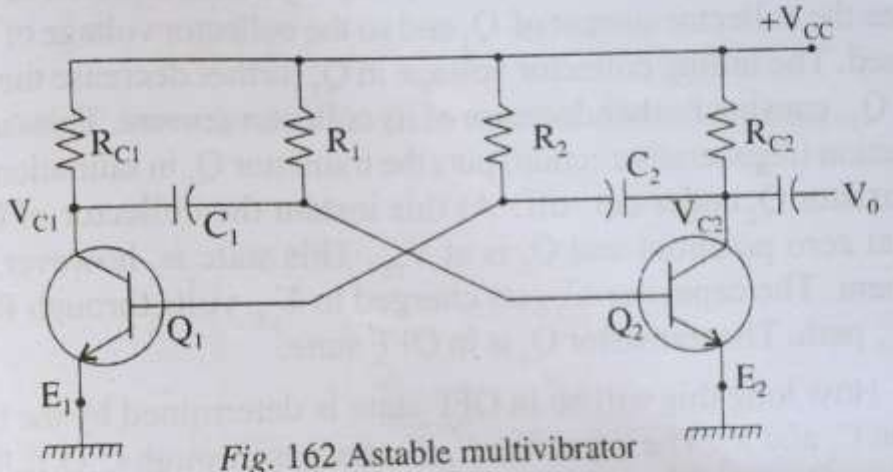


Fig. 162 Astable multivibrator

The circuit diagram of a free running multivibrator, in symmetric form, is shown in the figure. It is a two stage RC-coupled amplifier. The output of each stage is coupled to the input of the other through a capacitor (C_1 or C_2).

In the cross - coupling arrangement, each stage produces a phase change of 180^0 and hence the two inversions result in the positive feed back needed for oscillations. The amount of feed back is large enough to drive the transistors between cut-off and saturation conditions.

The resistance ratio (R_1 / R_C) is kept less than h_f (d.c. current gain) of the transistors used. The output will be available at the collector of either transistor in the form of pulses.

Working

When the circuit is switched on, the collector current flows through both the transistors. As the circuit is symmetrical, equal current flows through the transistors. But since two transistors are never identical, cur

rent through one of the transistors will be more. Let the current through Q_1 be slightly greater than that of Q_2.

Then the collector voltage of Q_1 is slightly less than that of Q_2. This causes decrease in the base current of Q_2, since the collector of Q_1 is coupled with base of Q_2 through C_1. As a result, the collector current of Q_2 is decreased and its collector voltage increases. This increases the base current of Q_1 because of the coupling capacitor C_2. This in turn, increases the collector current of Q_1 and so the collector voltage of Q_1 is decreased. The falling collector voltage in Q_1 further decrease the current of Q_2, causing further decrease of its collector current. This cumulative action (regenerative action) puts the transistor Q_1 in saturation and the transistor Q_2 under cut -off. At this instant the collector of Q_1 is nearly at zero potential and Q_2 is at V_{CC}. This state is, however, not permanent. The capacitor C_2 gets charged to V_{CC} volts through R_{c2} B $Q_1 E_1 R_{c2}$ path. The transistor Q_2 is in OFF state.

How long this will be in OFF state is determined by the time constant C_1 and R_1. The capacitor C_1 discharges through $C_1 Q_1 E_1 R_1 C_1$ path, since Q_1 is on. The discharge of capacitor C_1 causes the potential at A and hence at the base of Q_2 to rise above the cut-in voltage and makes the transistor Q_2 conducting. Due to regenerative action, Q_1 is at cut off and Q_2 is conducting. Eventually the capacitor C_1 gets charged to $+V_{cc}$ through R_{C1} $C_1 A Q_2 E_2 R_{C1}$.

As Q_2 is conducting, the capacitor C_2 discharges through $C_2 Q_2 E_2 R_2 C_2$ path, causing the potential at B and hence the potential of Q_1 to rise above the cut-in voltage. Due to regenerative action, Q_1 starts conducting (and the collector voltage decreases) and Q_2 is driven to cut off. The capacitor C_2 is recharged through R_{C2} $B Q_1 E_1 R_{C2}$ path again. The whole process is repeated.

Thus the transistors Q_1 and Q_2 are alternately switched on and off. The base of either of the transistors will show a negative r.m.s. voltage while the multivibrator is working. This is litmus test to see whether the circuit is working or not. The output taken from any one collector will be a square wave (pulse) and it will be complementary in time to the output from the other collector.

The period of the output wave is given by

$$T = 0.69\,(R_1C_1 + R_2C_2)$$

The frquency of the wave is

$$f = \frac{1}{T}$$

$$f = \frac{1}{0.69\,(R_1C_1 + R_2C_2)} \text{ hertz}$$

The output wave form is a square wave as shown in figure .

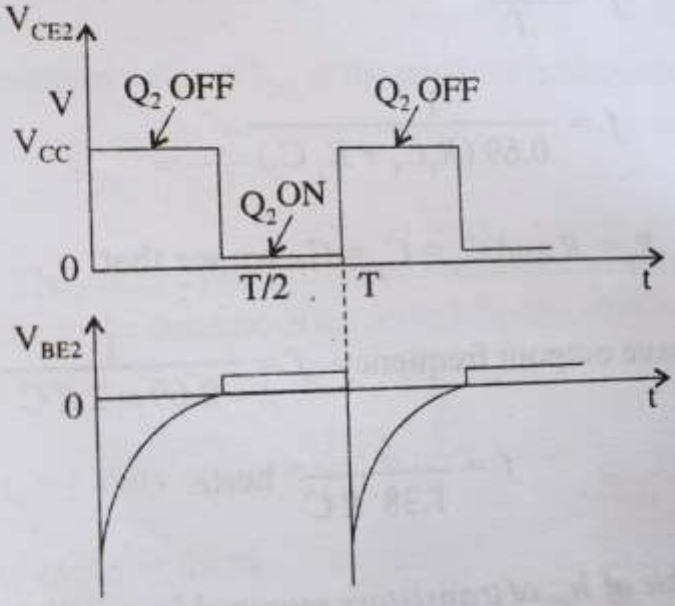


Fig. 163 Collector and base voltages of a transistor in a Astable multivibrator

Application of astable multivibrators

1. The astable multivibrator is used to produce a continuous train of square waves of rectangular pulses.

As a pulse generator, it is an important unit in digital electronics. The multivibrator serves as a reference clock to synchronize the timing in digital system for bringing about change of state of various (flip-flop) stages.

2. Since the output of the multivibrator is square waves, it is a source of production of harmonic frequencies of higher order. The circuit is often used for harmonic generation and because of this application, the circuit got the name *multivibrator*.

3. The astable multivibrator can be used along with logic gates to construct a digital voltmeter.

4. The output of a free- running multivibrator may be used to give the switching control at the base of power transistors in a d. c. - to - a. c. inverter. Similarly it can be used to operate at a higher frequency in a low - voltage - d. c. to higher - voltage - d. c. converter as in Switching Mode Power Supply (SMPS) used in T.V. set.

5. The astable multivibrator operates as an oscillator without the need for any input signal. It can be operated over a wide range of audio and radio frequencies. The frequency is determined by the time constants in the *RC* coupling circuits.

Thus, the multivibrator is a very compact circuit using transistors (or op-amp), resistors and capacitors but without the need for any coils or transformers for feedback.

Monostable multivibrator using transistors

As the name indicates, the monostable multivibrator is stable in just one state. It remains in its stable state until an input pulse triggers it into the other quasi stable state. It remains in that state for a time and then spontaneously will return to its initial stable state. The duration for which it remains in the quasi-stable state is determined not by the triggering signal but by the value of the components in the circuit itself. However, once the circuit returns to its stable state, it remains there until another trigger pulse arrives.

The circuit of a monostable multivibrator using transistors is shown in the figure. The base of transistor Q_2 is coupled to the collector of Q_1 through the capacitor C. The base of transistor Q_1 is coupled to the collector of Q_2 through the resistance R_2. A speed up capacitor C_2 (to reduce transition time) may be connected parallel to R_2. To keep Q_1 normally at cut-off, its base is connected to a negative voltage ($-V_{bb}$) through the resistance R_2. The output will be available at the collector of Q_2. Any input positive trigger pulse to produce change of state in the output should be applied to the base of Q_1 through the capacitor C_1.

Q_2 is normally ON because its base is biased to a positive voltage through R and only capacitor- coupled to the collector of Q_1. The capacitor C gets charged to V_{cc} volt through R_c. The charging path is V_{cc}, R_c, C, B_2, E_2, V_{cc}.

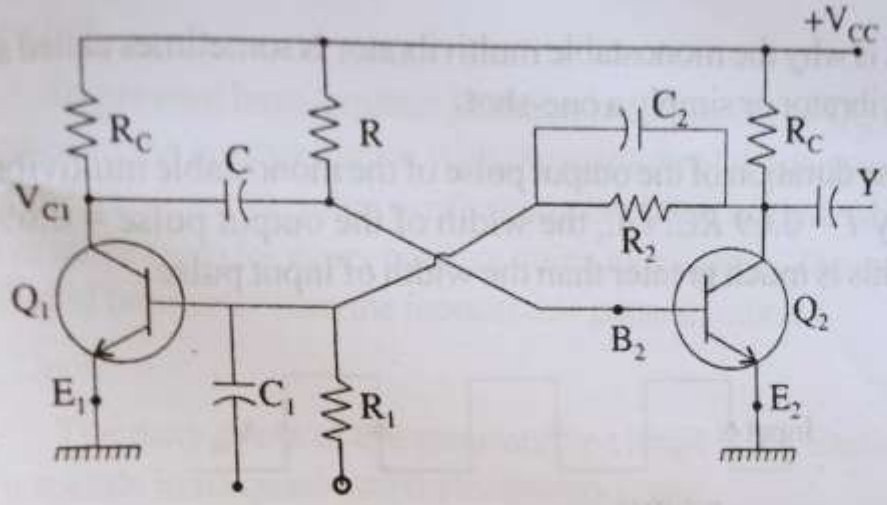


Fig. 164 Manostable multivibrator

Circuit operation and expression for width of output pulse

The circuit is triggered by applying a positive trigger pulse at the base of Q_1. This turns Q_1, ON, dropping the collector voltage of Q_1. Due to capacitor action, this drop is coupled to the base B_2, shutting the transistor Q_2 OFF, since its base- emitter junction becomes now reverse-biased, i.e., the circuit has gone to a quasi-state (with Q_1, ON and Q_2 OFF).

The condition Q_1, ON and Q_2 OFF is only temporary. As Q_1 is ON, the capactitor C discharges through it. The discharge path is C, Q_1, E_1, V_{CC}, R, C. As the capacitor charge in C changes due to discharging through R, reverse bias on the Q_2 base disappears. Upon reaching the cut-in voltages(0.7 V for silicon) the base - emitter junction of Q_2 becomes forward biased, preventing any further increase in potential. After an amount of time (T), determined by the RC time constant in the Q_2 base circuit, Q_2 again turns fully ON and Q_1 turns fully OFF. The circuit has switched over to its normal state.

Each time a positive pulse edge hits the Q_1 base, the output voltage goes from low to high temporarily and then returns to the low voltage. There is one rectangular pulse in the output for each triggering

pulse. This is why the monostable multivibrator is sometimes called a one shot multivibrator or simply a one-shot.

The duration of the output pulse of the monostable multivibrator is given by $T = 0.69\ RC$. i.e., the width of the output pulse = $0.69\ RC$ second. This is much greater than the width of input pulse.

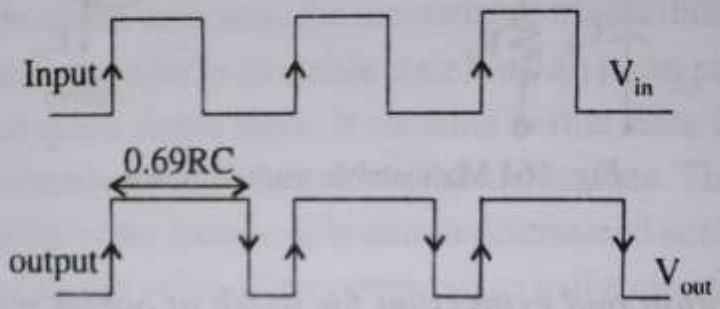


Fig. 165 Input - output wave forms of monostable multivibrator

The monostable waveforms

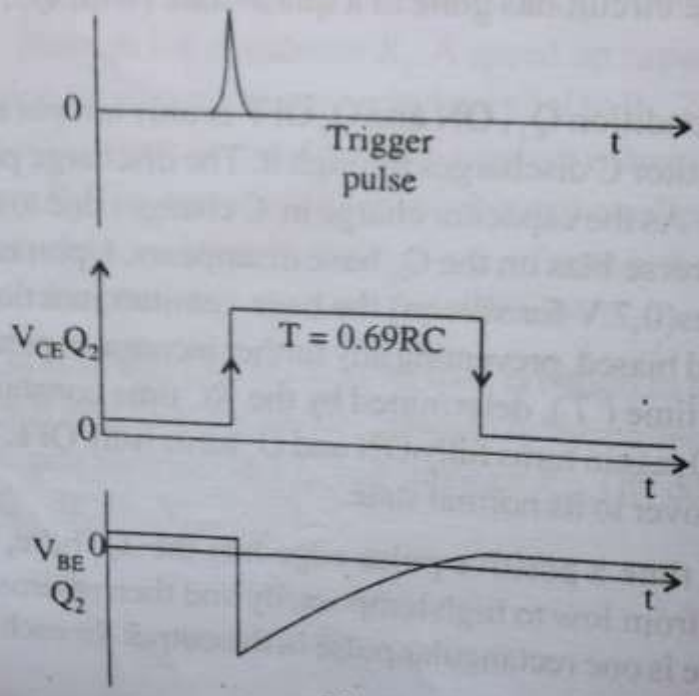


Fig. 166

Uses of monostable multivibrator

1. The monostable multivibrator can be used to function as an adjustable pulse width generator.

2. It is used as pulse shaper (to generate uniform width pulses from a variable width input pulse train). The mono-stable multivibrator can be used to re-generate old and worn- out pulses in computers and telecommunication systems. New clean and sharp pulses can be generated from out of the worn out pulses.

3. It is used as a time- delay unit since it produces a large output change (transition time) at a fixed time after the trigger signal.

Bistable multivibrator (Binary circuit - Flip Flop)

A bistable multivibrator or Flip Flop is one whose output is either a 'low' or 'high' voltage i.e., a 0 or a 1. This output stays low or high. To change the state of output, the circuit must be driven by an input, called trigger. Until the trigger arrives, the output voltage remains low or high indefinitely.

Figure shows the circuit of bi-stable multivibrator using transistors Q_1 and Q_2. The base of Q_2 is coupled to the collector of Q_1, through resistance R_1. Similarly, the base of Q_1 is connected to the collector of Q_2 through the resistance R_2. The base resistors R_3 and R_4 are connected to a common voltage - V_{bb} with respect to the common ground. The output signal will be made available at the collector of Q_2 or Q_1. The outputs

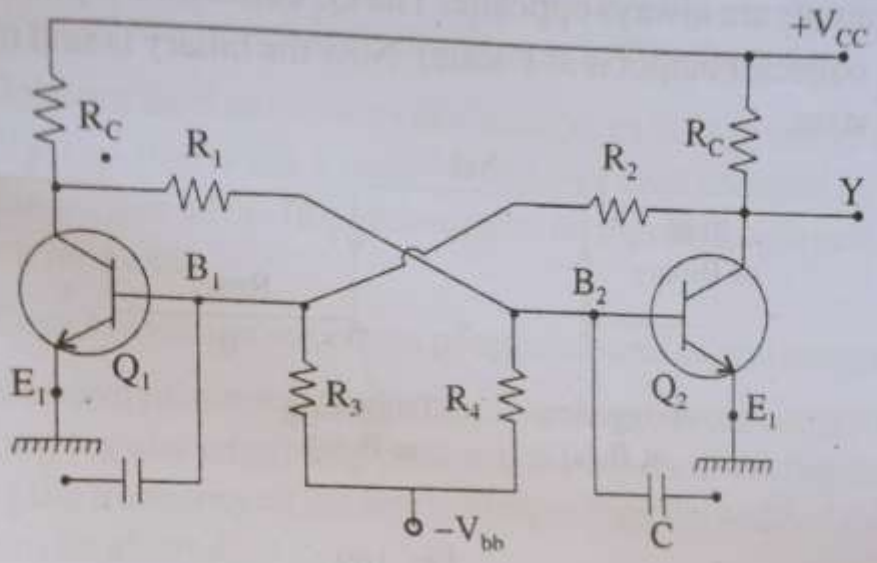


Fig. 168 Bistable multivibrator

at Q_2 and Q_1 will be complementary. Change of state in the output can be brought about by applying triggering pulse either at the terminal S (for Set) or at the terminal R (for Reset).

Working

The values of the resistors and the power supplies are so chosen that the transistors are forward biased at their base-emitter junctions (in spite of $-V_{bb}$). Both the transistors are in partially conducting state (in the amplification region).

A minute change in potential anywhere in the circuit may take the base of Q_2 more positive. Then Q_2 conducts more current and its collector voltage decreases. This decrease in voltage is coupled to the base of Q_1 through the potential divider consisting of R_2 and R_3. Hence Q_1 conducts less, causing an increase in its collector potential., This increase is coupled back to the base of Q_2 through the potential divider of R_1 and R_4. Hence Q_2 conducts more. The regenerative processes goes on until Q_2 becomes fully ON (saturation 0) and Q_1 becomes OFF (cut-off). This state of the binary is stable. In the stable state, the logic levels

at the outputs are always opposite. The Q_2 collector output is at 0 state (the Q_1 collector output is at 1 state). Now the binary is said to be in the Re-set state.

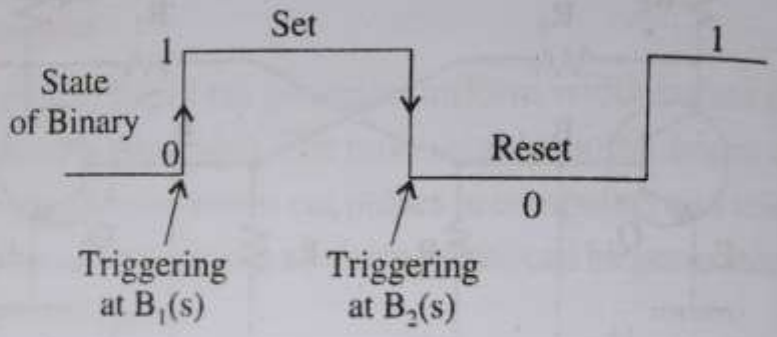


Fig. 169

To change the state of the binary (from 0 to 1 state) a positive trigger pulse is applied at the base of the Q_1 transistor. This positive pulse makes the transistor Q_1 to start conducting. As before, due to regenerative action Q_1 reaches saturation state and Q_2 will reach out-off state. This state is the other stable state of the binary. In this stable state, the output at Q_2 collector is 1 state. Now the binary is said to be in the set-state.

If a positive pulse is applied to the base of Q_2, the binary will be re-set. If the binary is already in the reset state, the triggering pulse at the base of Q_2 will not alter the state of the binary. Similarly, if the binary is already in the set-state, applying positive trigger pulse at the base of Q_1 will not change the state of the binary.

In practice, the positive pulse necessary for triggering can be produced using a 3 V battery, whose negative terminal is connected to the common ground of the binary circuit. A lead from the positive terminal is given a momentary contact at the base of the concerned transistor. One contact (pulse) at S flips the output at Q_2 collector to high state and the next contact at R flops the output back to low state and so on. The trigger pulses can also be produced by using separate pulse generator circuit.

Application of the bistable multivibrator (Flip-flop)

1. Flip-flops are used as memory devices (i.e, as storage units). Once the state of the flip-flop is set, it remains this way until changed by the next input pulse. Thus a flip-flop remembers its inputs. Logic gates do not have such memory.

2. Flip-flops are the nerve centres of registers and digital counters.

2. Flip-flops are the nerve centres of registers and digital counters.

3. Square wave of symmetrical shapes can be produced using flip-flops by sending regular triggering pulses to the inputs of the flip-flops. By adjusting the frequency of the input trigger pulses, the width of the square waves can be altered.

4. A flip-flop circuit can also be used as a frequency divider(as a divide - by two counter).

Schmitt trigger

Schmitt trigger is a wave shaping circuit that can convert a sine wave into a square wave.

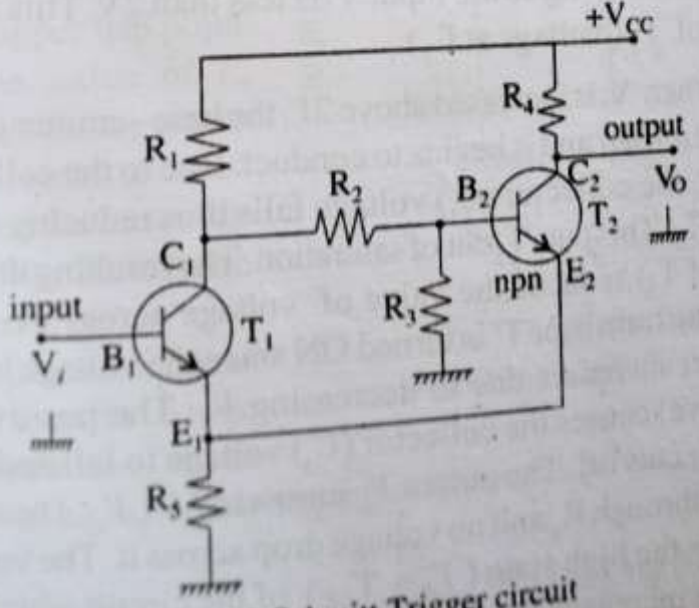


*Fig.*170 Schmitt Trigger circuit using transistors

The circuit makes use of two *n p n* transistors, whose emitters are connected together. The resistance R_5 is common to the emitters and it serves as the feedback path. This is unlike ordinary bistable circuit in which the collector of one transistor is connected to the base of the other. The resistors R_2 and R_3 form a potential divider arrangement to provide base bias voltage to the transistor T_2. The resistors R_1 and R_4 are load resistances in the two collector circuits. The input voltage is applied to the base (B_1) of T_1 with respect to the ground and the corresponding out put can be drawn from the collector (C_2) of T_2.

Action

When the input voltage $V_i = 0$, the transistor T_1 is off. Its collector voltage is V_{CC} (say 6V) and due to the potential divider arrangement with R_2 and R_3, the voltage supplied to the base (B_2) of transistor T_2 is sufficient to saturate T_2. Hence voltage V_{CE} between collector and emitter of T_2 becomes almost - zero. The supply voltage V_{CC} (say 6V) is dropped across the load resistance R_4 and emitter raistance R_5, in proportion to their ratio of resistances. Let us say, R_4 drops 4V and R_5 drops 2V. i.e. the T_2 collector to ground voltage is 2V i.e. the output = 2 volt. It will be always so, as long as the input V_i is less than 2V. This is the emitter potential of T_1 (voltage at E_1).

When V_i is increased above 2*V*, the base - emitter junction of T_1 is *forward biased* and it begins to conduct. Due to the collector current flow in R_1 the collector (C_1) voltage falls thus reducing the base (B_2) current in T_2. This puts T_2 out of saturation. The resulting drop in emitter current (of T_2) reduces the value of voltage across R_5, V_C As V_e is reduced, the transistor T_1 is turned ON since the voltage between base and emitter increases due to decreasing V_e. The positive feed back (regeneative) causes the collector (C_1) voltage to fall and T_1 saturates and now T_2 cuts off. The output V_o jumps to 6*V* (V_{CC}) because there is no current through R_4 and no voltage drop across it. The voltage at C_2 is V_{CC}. This is the high state ($V_o = V_{CC}$) of the circuit which is retained even if V_i is increased further. With T_1 saturated, V_e is only 1V (

kΩ, R_E = 1 kΩ

Current through transistor (T_1) circuit $= \frac{6V}{6\,k\Omega} = 1\,mA$

∴ Voltage across R_5 is $V_e = R_5 \times i_E = 1\,k\Omega \times 1\,mA = 1$ volt

To bring the circuit to the low state, the input V_i must be reduced so that T_1 comes out of saturation and returns to cut off condition. At the same time T_2 functions in the opposite way. As V_i is decreased, T_1 collector current decreases and the collector (C_1) voltage increases, thus causing transistor T_2 to conduct. This increases V_e and so T_1 collector current decreases further (since its emitter voltage has raised). This happens until the regenerative cuts off T_1 and saturates T_2. The condition now is the output $V_0 = 2$ volt (low state).

Characteristic graph (hysteresis behaviour)

The characteristic graph connecting input and output is shown in the figure.

The value of input V_i triggers the circuit and makes the output V_0 to jump from 'low' to 'high' state is called the upper trip point (UTP). The value of V_i which causes the oupput to jump from 'high' to 'low' state is called the lower trip point (LTP). Since the change from 'high' to 'low' state takes place at a lower value of V_i than the change in the reverse action (low to high), the circuit exhibits a lagging.or hysteresis effect in its switching action.

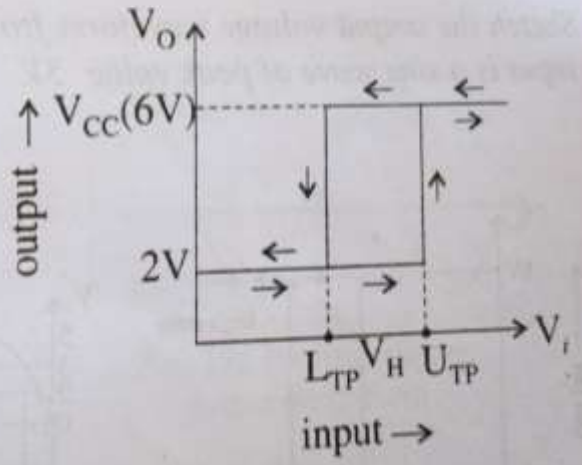


*Fig.*171 Schmitt Trigger circuit characteristics and hysteresis voltage

The UTP and LTP can be altered by changing the value of the emitter resistor R_e, thus giving different hysteresis range.

Uses of Schmitt trigger

The Schmitt trigger can be used

1. for generating square waves from sine waves
2. to get output pulses of uniform amplitude
3. as voltage comparators, which are useful in Analogue to Digital conversion
4. for detecting a signal whose strength exceeds a desired fixed voltage level.
5. for clipping waveforms.

Clippling circuit using diode (Limiter circuit)

A circuit with which the wave form of a signal may be shaped by removing a portion of the signal is known as clipping circuit or clipper (or limiter). ie, The clipper circuit removes or clips off part of a wave form above and /or below a specified level.

Principle

Diodes may be used as clippers or limiters. Because, diodes have very high resistance when they are off (for want of sufficient bias voltage). However, when a sufficiently large signal is applied across the diode, it will turn the diode on and the diode starts conducting. Any applied signal which is too small to forward bias the diode will not be affected by the diode.

(i) ***Positive Clipper***

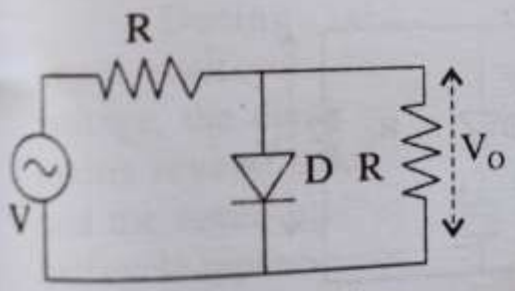


Fig. 174 Positive Clipper using a diode

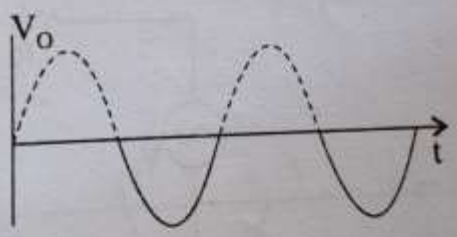


Fig. 175 Positive clipper output wave form

Figure shows a positive clipper, which removes positive part of the input signal. The input signal applied is a sine wave (shown by dotted line). During the positive half cycle of the input voltage, the diode conducts heavily (under forward bias condition) and it acts as a closed switch. The voltage across a short must be equal to zero. Hence the output voltage is zero during each positive half cycle. All the voltage is dropped across *R*.

During the negative half cycle, the diode is reverse biased and as looks open. No current passes through the diode, the circuit behaves as a voltage divider with R and R_L in series with the signal generator. The output voltage (across R_L) is

$$v_o = \frac{v_i \cdot R_L}{(R + R_L)}$$

If R_L is kept much greater than R, $R + R_L = R_L$

$v_o = -v_i$ since the positive half is clipped.

The input and output waveforms are shown in the figure. Similarly, by reversing the polarities of the diode, the negative half cycle of the input can be clipped. Such a clipper is known as negative clipper.

(ii) ***Biased Clipper***

In order to remove a small portion of positive or negative half cycle of the signal voltage, biased clipper is used.

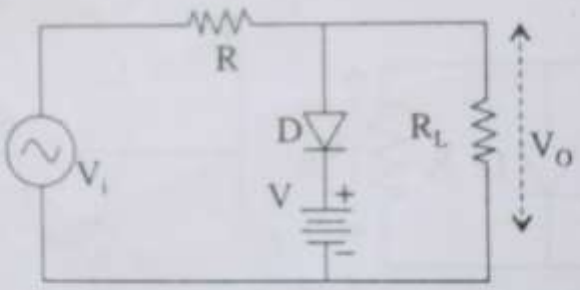


Fig. 176 Biased clipper circuit

The circuit shows a biased positive clipper with a battery of V volt in series with the diode. The combination is connected across the load resistance R_L. R is a limiting resistance in series with the input signal generator. It is assumed that the diode is ideal. (The ideal diode has zero current in reverse bias condition).

The diode will not conduct as long as the voltage at its anode is less than the battery voltage V. As the signal voltage begins to increase from 0 volt, nothing happens at first in the diode path since the diode does

(iii) *Combination clipper*

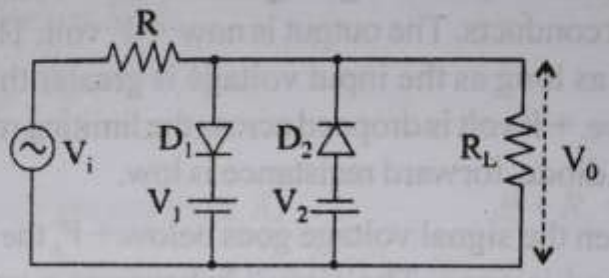


Fig. 178 Combination clipper circuit

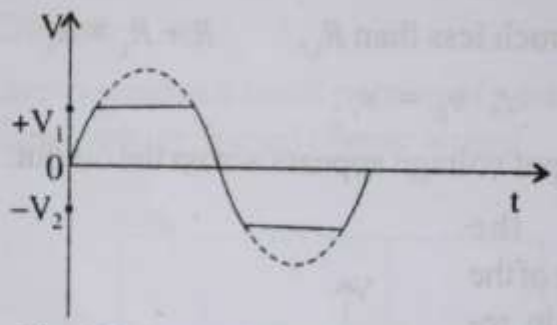


Fig. 179 Combination clipper output wave form

The circuit shows a combination of biased positive and negative clippers. A portion of both positive and negative half cycles of input voltage can be clipped using this circuit. The input voltage is a sine wave.

Action

When the input goes above the battery voltage V_1, the diode D_1 conducts heavily. But the diode D_2 remains reverse- biased. So, a voltage $+V_1$ appears across the load, as long as the input- voltage is more than $+V_1$.

During the negative *half* cycle the diode D_2 will conduct heavily and the output remains at $(-V_2)$ so long as the input voltage is more negative than $(-V_2)$. When the input voltage lies between $+V_1$ and $(-V_2)$, neither diodes is on. With R_L much greater than R, the input voltage appears across the output when the input sine wave signal is larger than the clipping level, the output resembles a square wave.

Applications of clippers

1. With sine wave input signal, square waves can be produced using combination clippers.

2. The limiting action of the clipper may be used to limit a signal when it is too large. For example, clippers can be used to keep audio signals from exceeding certain loudness limit.

3. Clippers can be used to remove noise pulses, riding on a signal. If the noise pulses exceed the clipping point, then they will be clipped off and the resulting signal will be noise-free than the original.

Clamping circuit using diodes (level shifter)

A circuit, that enables to shift a given signal vertically through a desired voltage level, preserving the shape of the orginal signal, is known as a clamper (or d.c. restorer) ie, the clamper circuit adds a de level to an ac voltage using a diode and a capacitor.

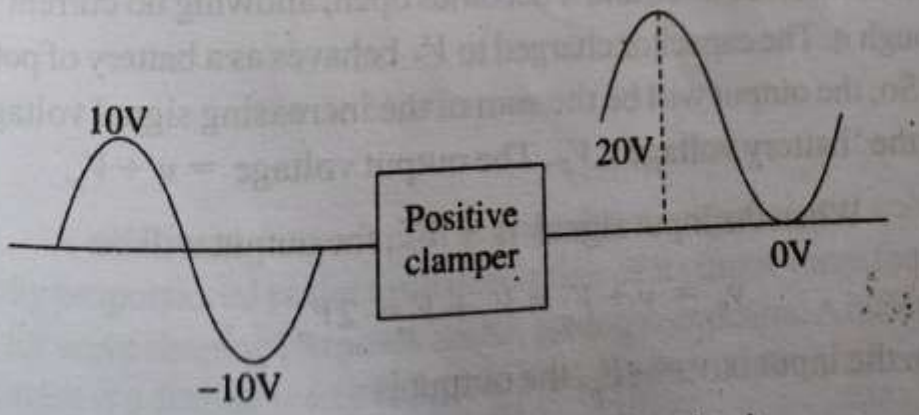


Fig. 180 Positive clamping circuit
input - output wave form

(i) *Positive clamper*

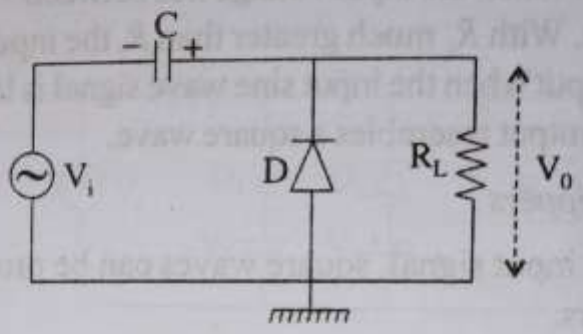


Fig. 181 Positive clamper

The *circuit consists* of a diode D and a capacitor C in series with a signal source that generates an a.c. wave form. The load resistance R_L is connected paralled to the diode. The clamped output signal is made available across the load R_L.

The *circuit action* is as follows: During the first negative cycle of the input signal, the diode is forward biased and it conducts heavily. At the negative peak of the input, the capacitor is fully charged to its peak voltage V_P, with the polarities shown in the figure.

Slightly beyond the negative peak (ie, at positive going) the diode is reverse biased and it becomes open, allowing no current to pass through it. The capacitor charged to V_P behaves as a battery of potential, V_P. So, the output will be the sum of the increasing signal voltage (v) and the 'battery voltage', V_P. The output voltage $= v + V_P$.

When the input signal is $+ V_P$, the output will be

$$v_0 = v + V_p = V_p + V_p = 2V_p.$$

When the input is $v = -V_p$, the output is

$$v_0 = v + V_p = -V_p + V_p = 0$$

Thus, the signal varying from $-V_p$ to $+V_p$ is available across the load as a signal whose strength varies from 0 to $2V_p$. Obviously there is a positive level shifting of V_p volt in the output, when compared to the input.

A negative clamper can be constructed by reverse connecting the diode in its place in the circuit. In this case, there is a level shifting of the input signal through $(-V_p)$. The output is

$$V_0 = v - V_p,$$

causing a voltage swing between 0 and $-2V_p$.

Application

Both positive and negative clampers are widely used. For example, television receivers use a clamper to add a d.c. voltage to the video signal. Clamping circuits canbe used as voltage doublers or voltage multipliers.

Differentiating circuit using passive elements

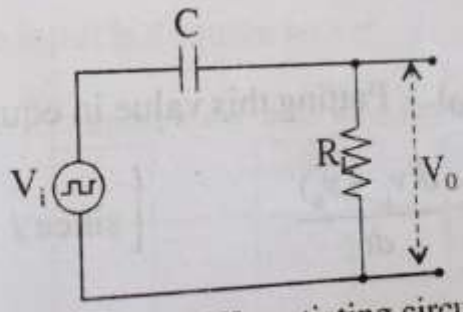


Fig. 182 Differentiating circuit

A differentiating circuit is one whose output signal voltage is directly proportional to the time derivative of its input wave form. It is used for wave shaping purposes and in analog computers. A differentiating circuit is a simple series RC circuit where the output is taken across the resistor R.

The differentiating circuit consists of a capacitance C and a r sistance R connected in series with the signal generator (of low fre

quency). The output v_0 is drawn from across R. Let us assume that the value of R is very small, when compared with the reactance $(1/C\omega)$ of the capacitor at the highest frequency of the input wave, for which the circuit is designed.

Let v_i be the input signal voltage (that may be a square wave or triangular wave). Let v_0 be the output signal voltage. If i be the current through the circuit at any instant t

$$v_0 = i \times R \qquad \text{.....(1)}$$

Since the current is the rate of flow of electric charge, $i = dq/dt$

$$v_0 = R \cdot \frac{dq}{dt}$$

To find dq : From the definition of capacitance,

$C = \frac{dq}{dv}$ where v is the voltage across the capacitor, $v = (v_i - v_0)$

$$C = \frac{dq}{d(v_i - v_0)}$$

$\therefore dq = C.d(v_i - v_o)$. Putting this value in equation (1),

the output $v_0 = RC\frac{d(v_i - v_0)}{dt}$ $\left[\text{since } i = \frac{dq}{dt}\right]$ .....(2)

Since $R < 1/C\omega$, the voltage across R is very much smaller than the voltage drop across the capacitor. $v_0 < v_i$

$\therefore v_i - v_o \simeq v_i$. Using this in equation (2),

the output $v_0 = (RC)\frac{dv_i}{dt}$

The quantity (RC) is the time constant of the circuit and it is of fixed value.

$\therefore$ The output voltage $v_o \propto \frac{dv_i}{dt}$

i.e., the output voltage is proportional to the time derivative of the input signal. That is, the output wave form which depends on how fast the input voltage changes. Because of this ability to differentiate between the rates of change of applied voltage, the circuit is called differentiator circuit.

In order to get good differentiation, the following two conditions should be satisfied : - (1) The time constant (RC) must be smaller than the period of the input wave form since we have assumed $R < 1/C\omega$ in the derivation.

ie., $R < 1/C\omega$; $RC < 1/\omega$; $RC < T/2\pi$

$\therefore RC < T$, where T is the period of the input signal.

(2) The value of the reactance of the capacitor ($X_C = 1/C\omega$) should be 10 or more times larger than the value of R at the operating frequency (of the input signal).

Special cases

Case 1 : When the input is a square wave:

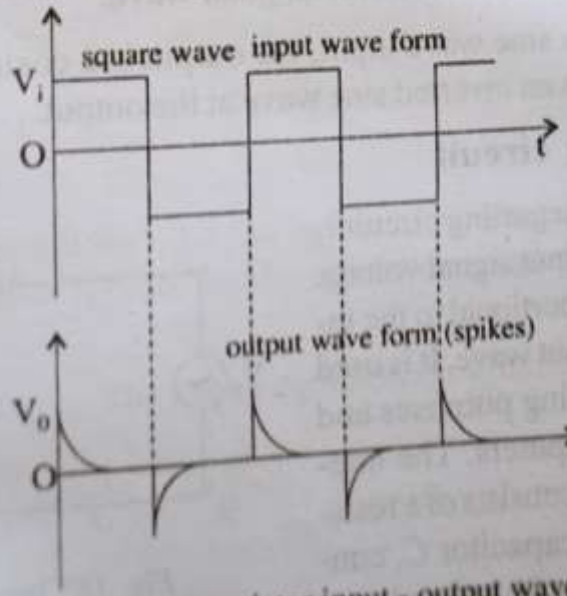
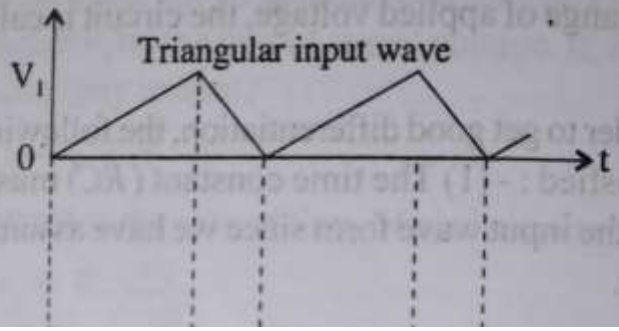


Fig. 183 Differentiator input - output wave forms (spikes)

For the square wave input, the output is a series of sharp spikes. Sharp spikes are produced due to short time constant (RC) of the circuit. Such sharp spikes are used to trigger multivibrator circuits of counters.

Case 2 : When the input is a saw tooth wave



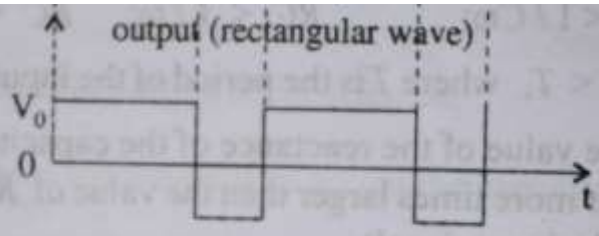


Fig. 184 Differentiating circuit output for triangular input wave

The output, in this case, is a rectangular wave.

Case 3: For a sine wave input, the output is a cosine wave. A cosine input becomes an inverted sine wave at the output.

Integrating circuit

An integrating circuit is one whose output signal voltage is directly proportional to the integral of its input wave. It is used for wave shaping purposes and in analog computers. The integrating circuit consists of a resistance R and a capacitor C, connected in series with a signal generator of high frequency. The output v_o is drawn from across C.

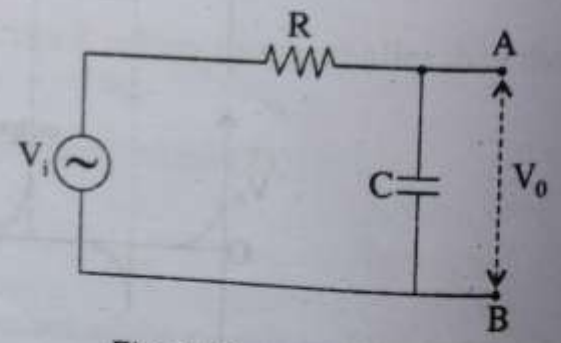


Fig. 185 Integrating circuit

Let us assume that the value of the reactance of the capacitor ($1/C\omega$) is much smaller when compared to the resistance R at the lowest frequency of the input wave, for which the circuit is designed.

Let v_i be the input signal voltage and v_0 be the output signal voltage. If i be the current in the circuit,

$$v_i = v_o + R_i$$

$$\therefore\ i = \frac{(v_i - v_0)}{R} \qquad \text{.....(1)}$$

From the definition of capacitance, $C = \frac{dq}{dv}$ $\qquad (Q = CV)$

where v is the voltage across the capacitance. Since $dq = i.dt$,

$$C = i\frac{dt}{dv}$$

$$\therefore\ dv = \frac{i\,dt}{C} \qquad \text{..... (2)}$$

By integrating the above, the output voltage v_0 can be obtained.

$$v_0 = \int dv = \int \frac{i\,dt}{C} \quad \text{using equation(2)}$$

$$v_0 = \frac{1}{C} \int \frac{(v_i - v_o)}{R} . dt \quad \text{using equation (1)}$$

Since we have assumd that $1 / C\omega$ is much less than R, the voltage across the capacitance is much smaller than the voltage drop across the resistance.

ie., $v_o << v_i$ The above equation for v_o becomes

$$v_o = \frac{1}{C} \int \frac{v_i\,dt}{R}$$

$$v_o = \frac{1}{CR} . \int v_i\,dt$$

where $(C R)$ is the time constant of the circuit, which is of fixed value.

$\therefore$ output voltage $v_o \propto \int v_i\,dt$

Thus, the output voltage is proportional to the integral of the input voltage over the time for which the input is active. In this case, the time constant (RC) should be high enough to get good integrated output wave. For the integrator to work properly, the time constant must be greater than the width (T) of the input pulse. Roughly, $RC > 10\,T$.

Special Cases

Case 1: When the input is a square wave, the output will be a triangular wave.

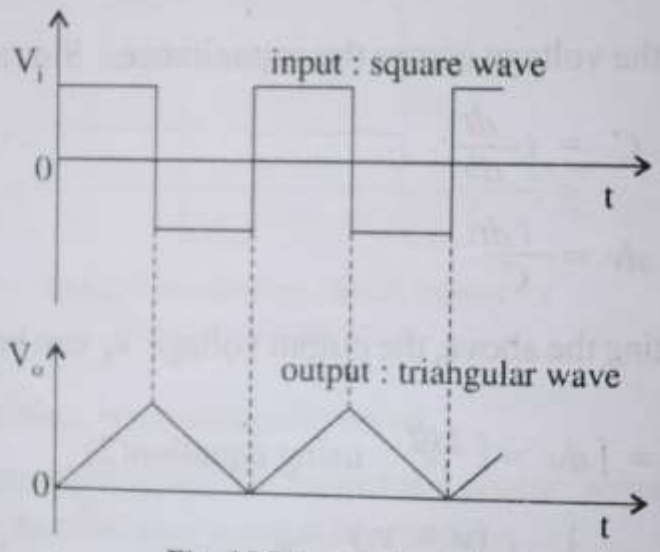


Fig. 186 Integrating circuit : input - output wave form

Case 2 : When the input is rectangular wave, the output will be a saw-tooth wave.

Applications

R C integrators are frequently used in electronic systems : for example, in automatic gain control, detector and filter. Because of its slow response to voltage changes, the integrator can also be used as a pulse delay network. Integrators are also used as phase changers and low pass filters.

Questions

1. Explain positive and negative feedback. Where are they applied?
2. What are the advantages of negative feedback?
3. How does an oscillator differ from an amplifier?
4. Explain the principle of negative feedback in an amplifier. Derive an expression for voltage gain with negative feedback.
5. What is a tank circuit? What are the functions of tank circuit in an oscillator?
6. Draw the circuit diagram of Colpitt's oscillator using transistor. Explain its working and derive an expression for frequency of oscillation and also find the condition for oscillations to start.
7. What are sinusoidal oscillators? Give two examples, with their circuit diagrams.
8. Draw the circuit diagram of Hartley oscillator and explain its working. Derive the condition for oscillation and expression for frequency of oscillation.
9. Draw the circuit diagram of phase shift oscillator using transistor and explain its working. Obtain the minimum gain necessary for oscillations to start and deduce the expression for frequency of oscillations.
10. Explain the functions of ladder net work in phase shift oscillator. Derive expressions for frequency and minimum gain required for oscillation.
11. What are multivibrators? Describe the function of astable multivibrator using transistors. Sketch the output waveform. Arrive at an expression for frequency of the astable multivibrator and its duty cycle.

12. Describe the applications of (1) astable multivibrator (ii) monostable multivibrator and (iii) bistable multivibrator.

13. Explain, giving circuit diagram, the working of monostable multivibrator using transistors.

14. Draw the ciruit diagram of bistable multivibrator and explain its action.

15. Draw the circuit diagram of a Schimitt trigger using transistor. Explain its working. Describe its hysteresis behaviour. What are the uses of Schimitt trigger?

16. What are clipping circuits? Explain the action of a combination clipper. What are the applications of clipping circuit?

17. What are clamping circuits? Explain the action of a positive clamper. What are the applications of clamping circuits?

18. What are differentiating and integrating circuits? Obtain expression for output voltage in each case. Mention the applications of differenciating and integrating circuits.

Objective type questions

1. An oscillator is an amplifier with
   (a) positive feedback (b) negative feedback
   (c) neither (a) nor (b) (d) R.C. network
2. Negative feedback
   (a) lowers the gain (b) improves stability
   (c) increases the input impedance (d) all the above
3. Barkhaussen criterion for oscillation is
   (a) $A\beta = 1$ (b) $A\beta > 1$ (c) $A\beta < 1$ (d) $A\beta = -1$
4. An oscillator converts
   (a) a.c. power into d.c. power
   (b) d.c. power to a.c. power
   (c) mechanical power into a.c. power
   (d) generates power

6. In Colpitt's oscillator, the feedback is

(a) inductive (b) capacitive

(c) resistive (d) all the above

7. In Hartley osillator, the feed back is

(a) inductive (b) capacitative

(c) resistive (d) all the above

8. In a certain oscillator, gain $A_v = 50$. The feedback ratio should be

(a) 1 (b) 0.01 (c) 10 (d) 0.02

9. In a Hartley oscillator, the value of L is increased 4 times, the frequency of oscillation is _____.

(a) increased 2 times (b) decreased 4 times

(c) increased 4 times (d) dercreased 2 times

10. The voltage that starts on an oscillator is caused by

(a) ripple voltage from power supply

(b) noise voltage in resistors

(c) input signal from a voltage generator

(d) positive feedback

11. In the feedback path of phase shift oscillator, each RC section produces phase shift of about

(a) 180^0 (b) 90^0 (c) 60^0 (d) 30^0

12. The minimum gain required for oscillation in phase shift oscillator is

(a) h_{FE} (b) –29 (c) 1 (d) –26

13. The oscillator that gives the most stable output is

(a) Hartley oscillator (b) Colpitts oscillator

(c) phase shift oscillator (d) crystal oscillator

14. In a multivibrator, the operating point moves between

(a) cut off and saturation (b) cut off and active region

(c) active region and saturation (d) none of the above

15. An oscillator converts

(a) d.c. power into a.c. power

(b) mechanical power into a.c.power

(c) a.c. power into d.c. power

(d) all the above

16. The multivibrator used for harmonic generation of square waves is

(a) monostable (b) bistable

(c) astable (d) all the above

17. Multivibrator, used as memory device, is

(a) Monostable (b) bistable

(c) astable (d) all the above

18. In a multivibrator, the feedback is

(a) 100 % positive (b) negative

(c) both positive and negative (d) all the above

19. Negative current feedback in amplifiers

(a) increases voltage gain

(b) decreases voltage gain

(c) does not affect voltage gain

(d) first decreases and then increases the voltage

Answers

1. (a)	2. (d)	3. (a)	4. (b)	5. (a)	6. (b)	7. (a)
8. (d)	9. (d)	10. (b)	11. (c)	12. (b)	13. (d)	14. (a)
15. (a)	16. (c)	17. (b)	18. (a)	19. (c)		

UNIT-V

OPERATIONAL AMPLIFIER

Op-Amp - pin diagram- characteristics of ideal Op - Amp - DC and A.C analysis - bandwidth - slew rate - frequency response - Op- Amp with negative feedback - applications - Inverting amplifier - Non inverting amplifier - Voltage follower- Adder - Subtractor - Integrator – Differentiator- Low pass, High pass and Band pass filters -Wien bridge oscillator.

Differential Amplifier

Differential amplifier is used as the first stage of integrated circuit operational amplifiers. Figure shows the basic circuit diagram of a differential amplifier.

The amplifier makes use of two identical transistors, whose collectors are connected to power supply $+V_{CC}$ (with respect to ground), through identical resistors R_C and R_C as in figure. The emitters are connected together to one end of a resistor R_E, whose other end is connected to power supply $-V_{EE}$ with respect to ground. v_1 and v_2 are two inputs given to bases of the two transistors and v_0 is the output, which is made available across the collector terminals.

The output $v_0 = (v_{c1} - v_{c2})$

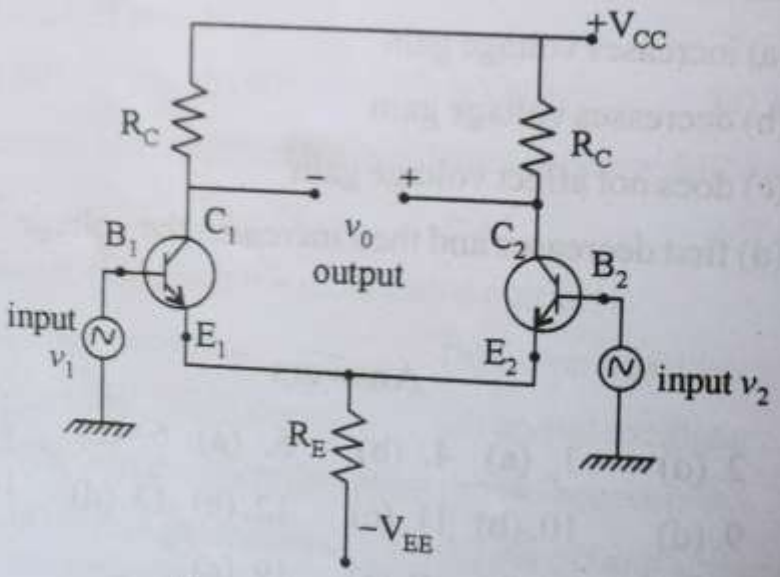


Fig. 187 *Differential amplifier.*

(i) Differential mode operation

Two input signals are applied. The input voltage v_1 is called non-inverting input because the output v_0 is in phase with v_1. The input v_2 is called inverting input because v_0 is 180° out of phase with v_2. When both the inputs are applied, the total input is called differential input, which is $(v_1 - v_2)$. If A be the voltage gain, the output is given by

$$v_0 = A\,(v_1 - v_2)$$

This output is the differential output and the gain A is known as the differential gain, A_d.

(ii) Common-mode operation

Here, two in-phase signals are applied to the bases as inputs at the same time. The input is known as common mode input. The transistors are now operating in parallel. Let V_S be the common applied signal. Then, the total emitter current *change* is given by

$$\Delta I_E = \frac{V_S}{R_E} \qquad \ldots\ldots (1)$$

The emitter current divides into two branches equally.

$\therefore$ the emitter current change in each transistor is

$$\Delta I_{E1} = \Delta I_{E2} = \frac{\Delta I_E}{2}$$

Using equation (1),

$$\Delta I_{E1} = \Delta I_{E2} = \frac{V_S}{2R_E} \qquad \ldots\ldots (2)$$

$\therefore$ The collector current change is

$$\Delta I_C = \Delta I_{E1}$$

$$\Delta I_C = \frac{V_S}{2R_E} \quad \text{using equation (2)}$$

If ΔV_C is the voltage change at transistor collectors,

$$\Delta V_C = -\Delta I_C \times R_C$$

$$\Delta V_C = -\frac{V_S}{2R_E} \times R_C$$

This gives the output voltage change ΔV_o

i.e; $$\Delta V_o = -\frac{V_S}{2R_E} \times R_C$$

$$\therefore \quad \frac{\Delta V_o}{V_S} = -\frac{R_C}{2R_E}$$

This gives the common mode gain A_C.

$$\therefore A_C = -\frac{R_C}{2R_E}$$

Knowing R_C and R_E in the circuit, the common mode gain A_C can be calculated.

A good amplifier should reject common mode input signals in the output. i.e., A_C must be a small as possible. This might be achieved by increasing the value of the emitter resistance R_E. But this will reduce the value of d.c. emitter and collectr currents. This can be overcome by including a *constant-current tail* (with another transistor) in the emitter circuit. The ratio (A_d/A_c) is called common mode rejection ratio (CMRR)

(iii) Performance

1. This differential amplifier has high input impedance and high voltage gain.
2. Direct coupling is used and there is no need for emitter by-pass capacitors and hence there is no lower cut-off frequency.
3. The differential amplifier has *excellent bias stability* as it uses emitter bias, where the emitter current I_E is independent of transistor h_{FE} variations.

Amplifier

An amplifier is an electronic device that enlarges small signal voltages applied to it. Amplifiers make sound louder and signal levels greater, by providing gain. The essential parts of an amplifier are (i) an active device like transistor (ii) input signal to be amplified and (ii) a.d.c. power supply

to actuate the active device. The input signal is an electrical quantity (voltage) that is too small in its present form to be usable. With gain, it becomes usable. The output signal is greater than the input because of the gain of the amplifier.

To obtain larger gains, two or more amplifiers are connected one after another (cascaded). There are different methods of coupling successive stages of a cascaded amplifier such as resistance-capacitance (R.C) coupling, L.C. coupling, transformer coupling, and direct coupling.

Differential amplifier

A differential amplifier amplifies the difference between two signals. Figure shows the *block diagram* of a differential amplifier with two input terminals and one output terminal.

If V_1 and V_2 are the input signals and V_0 the output signal, each measured with respect to ground, then

$$V_0 = A_V(V_1 - V_2)$$

where A_V is the gain of the differential amplifier. The output is proportional to the *difference* between the two input signals.

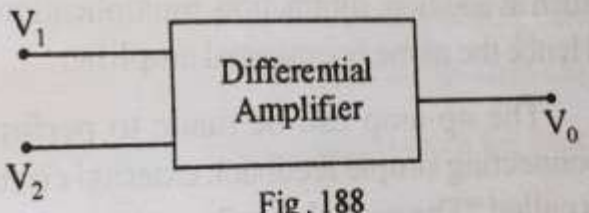


Fig. 188

A circuit with two transistors (CE amplifiers) having their emitters coupled to a common resistance (whose lower end is earthed) forms a differential amplifier. Such a circuit has high input impedance and high voltage gain.

The differential amplifier is the basic stage of an integrated operational amplifier (op-amp).

Operational amplifier

An operational amplifier (op-amp) is a high gain, direct coupled amplier. It is designed to amplify a.c. and d.c. signal voltages. Since the op-amp is used to amplify d.c. voltages also, the op-amp uses direct coupling throughout.

However, the op-amp is not made up of discrete components but is

an integrated circuit (*I.C.*) in a single-chip. Here the passive and active components needed to form the cascaded amplifier are diffused and then interconnected in a monolithic (single crystal) silicon chip.

The different stages of the operational amplifier are shown in the block diagram given below.

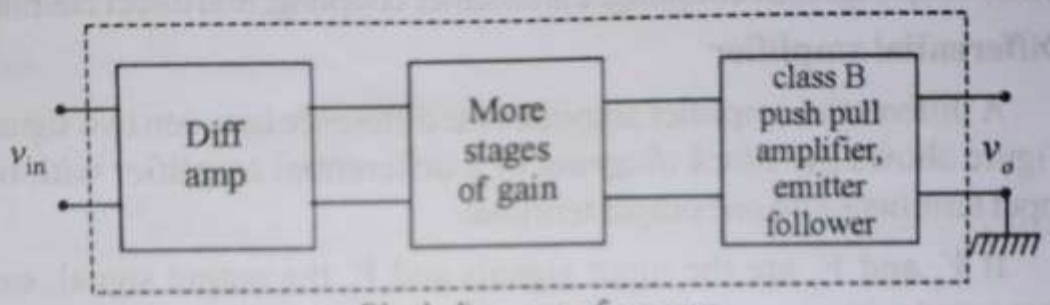


Fig . 188 *Block diagram of op amp.*

The basic function of an op-amp is to produce amplification. Apart from that, op-amp can also be used to perform mathematical operations such as addition, subtraction, multiplication, integration, differentiation etc. Hence the name operational amplifier.

The op-amp can be made to perform the desired operations by connecting simple feedback external circuit. For this reason the op-amp is called "The work-horse".

Whenever an op-amp is to be used, it is seldom necessary to show the details of the internal circuitry. Rather, it is enough to identify the terminals for the external circuitry.

A.C. and d.c. analysis of op-amp and equivalent circuit

Figure shows reduced block diagram of a typical op-amp. There are two inputs, labelled V_1 and V_2. The input voltages are V_1 and V_2 with

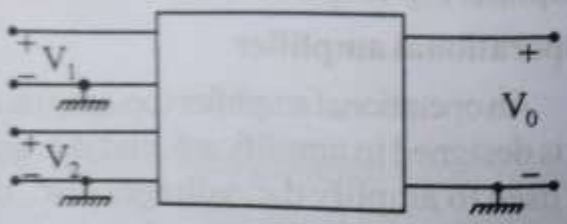


Fig . 189

respect to the ground. The output voltage is V_0 with respect to the ground. The output is given by

$$V_0 = A_V (V_1 - V_2)$$

where A_V is the voltage gain of the op-amp. A_V is assumed to be negative for the differential input $V_1 - V_2$. It is seen that V_0 is proportional to negative of V_1. Hence, a signal applied as V_1 is inverted (180° phase change) at the output. So V_1 is called the inverting input. It is denoted by a negative sign at the termianl in the block diagram.

Any signal applied as the other input voltage V_2 produces an output proportional to V_2 and is in phase with it. Hence V_2 is called the non-inverting input. It is denoted by 'plus' sign at the terminal in the block diagram.

It is also seen that one lead is common to both the inputs and the output. This is the ground lead. Since the ground lead is common to all ports of the circuit, it is often not shown in diagrams. For using an op-amp, it must be connected to a dual power supply (having $+V_{CC}$ and $-V_{CC}$) with respect to the common ground. The actual op-amp chip has leads for the power supply. These are often omitted from the block

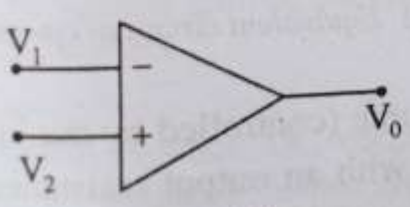


Fig. 190

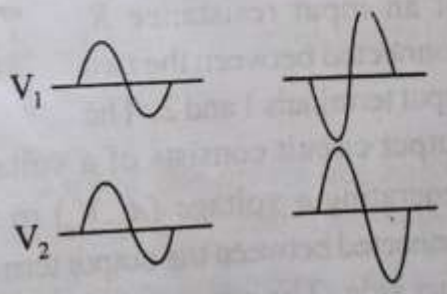


Fig. 191

diagram as in fig.

The function of the op-amp described above can be summarised as follows:

Differential input $V_d = (V_1 - V_2)$ is positive: the output is negative.

Differential input $V_d = (V_1 - V_2)$ is negative: the output is positive.

Ac analysis of op-amp

Equivalent circuit of an op-amp

Consider the schematic diagram of an op-amp as in fig. If V_1 and V_2 are the inverting and the non-inverting inputs, the differential input $V_d = (V_1 - V_2)$.

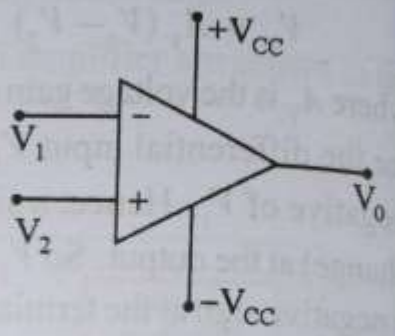


Fig. 192

If A_V is the voltage gain of the amplifier, the output voltage V_o with respect to ground is

$$V_o = A_V \times V_d .$$

When $V_2 = 0$ (grounded), the output $V_o = A_V . V_1$

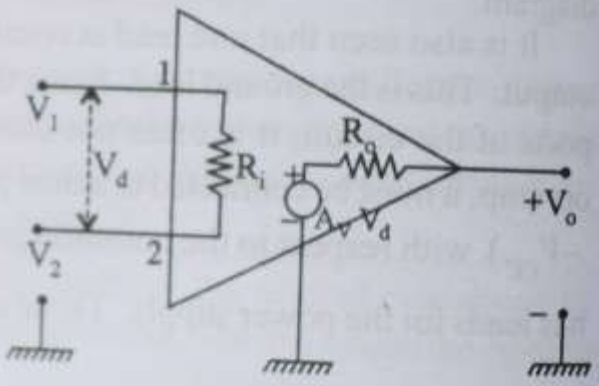


Fig. 193 *Equivalent circuit of op-amp.*

The a.c. equivalent circuit of an op-amp consists of an input resistance R_i connected between the two input terminals 1 and 2. The output circuit consists of a voltage source (controlled by the input) generating a voltage $(A_V V_d)$ in series with an output resistance R_o connected between the output terminal on one side and the ground on the other side. The output is measured with respect to ground.

Characteristics of an ideal op-amp

1. The input resistance is infinity *i.e.*, $R_i = \infty$. The input resistance is the resistance offered by the device as seen by the source, providing the input.

$$R_i = \frac{\text{input voltage change}}{\text{input current change}}$$

Since R_i is infinity, the op-amp draws no current from the source *i.e.*, the ideal op-amp does not load the source.

2. The output resistance is zero *i.e.*, $R_o = 0$

The output resistance is the resistance offered by the device as seen by the load

$$R_o = \frac{\text{output voltage change}}{\text{output (load) current change}}$$

Since $R_o = 0$, the ideal op-amp can supply maximum current to the load, irrespective of the value of the load.

3. The voltage gain is infinity, $A_v = -\infty$

Here, by A_v we mean the *open-loop gain* of the op-amp *i.e.*, without the use of any external feedback circuit. Since A_v is very large, even a feeble differential input signal (of the order of nanovolt) gets amplified to a large extend (to the order of volt) quickly.

4. The band width is infinity.

The voltage gain of the amplifier is canstant at *all frequencies* of the input signals.

5. Perfect balance *i.e.*, output $V_o = 0$ *when the inputs are equal* ($V_1 = V_2$). Any signal, common to both the inputs, is rejected at the output.

6. The characteristics do not drift due to variations in temperature. These characteristics are never realised in actual practice but they help to analyse op-amp circuits easily.

7. Slew rate is infinity. ie. the output changes according to the change in input without any delay.

Op-amps are fabricated in integrated circuit (IC) to achieve the above said ideal properties.

Common mode rejection ratio (CMRR)

To express how successful an amplifier is, in providing gain for the differential signal and rejecting the common mode signal, a factor called the common mode rejection ratio (CMRR) is used. It is defined as follows:

$$\text{CMRR} = \frac{\text{differential gain } A_d}{\text{common - mode gain } A_C}$$

Practical operational amplifier

The op-amps are fabricated in integrated circuit (IC) form to achieve the above said ideal properties. In actual practice, these properties are never realised

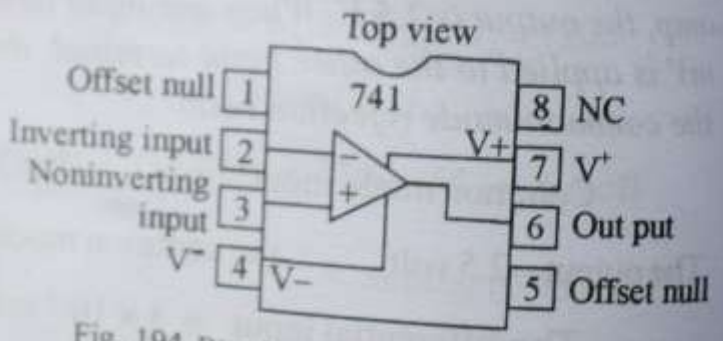


Fig. 194 *Pin diagram : 8 pin dual-in-line*

i.e., the voltage gain $A_v \neq -\infty$

the input resistance $R_i \neq \infty$

the output resistance $R_o \neq 0$ and so on.

In the ideal op-amp, the output will be a linear function of the differential input,

$$V_o = A_d (V_1 - V_2).$$

Now $V_o = A_d V_d$, where A_d is the differential gain of the op-amp and differential input $V_d = V_1 - V_2$.

In the actual op-amp, the response is not exactly linear. It is *nearly* linear over a region in which the value of $(V_1 - V_2)$ is small. Moreover, the output also consists of an error term due to the common mode input voltage,

$$V_C = (V_1 + V_2)/2$$

In this case, the output $V_o = A_C V_C$ where A_C is the common mode gain.

Pin diagram

Of the different types of op-amps produced, op-amp 741 type is widely used. The IC 741 operational amplifier looks like a small chip.It is available in 14-pin dual-in-line. 8pin dual-in-line (Fig. 170) or in TO-style packages (Fig.). The pin configuration of the 8 pin packages are shown in figure.

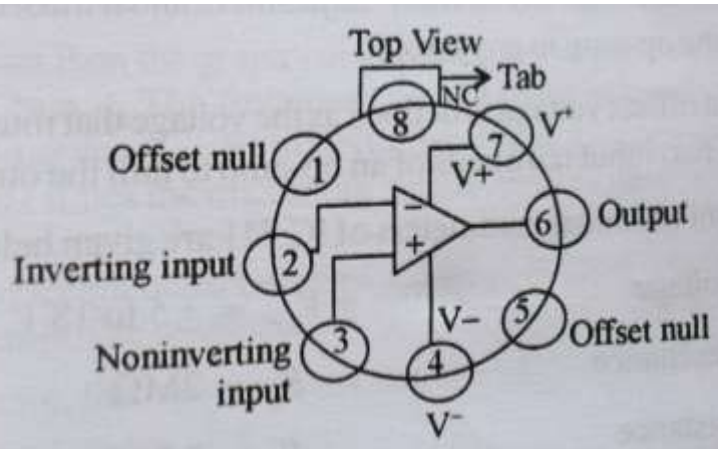


Fig. 195 *Pin diagram : 8 pin TO-style package.*

The operational amplifier needs a dual symmetrical power supply ($+V_{CC}$ and $-V_{CC}$) with the center tap of the power transformer secondary earthed. This earth is used as the common earth for all voltage sources in the circuit.

The op-amp circuit is designed to give zero d.c. output voltage when both the inputs V_1 and V_2 are earth-connected. However, because of small internal unbalances in some cases, a small d.c. voltage may appear at the output. This can be set to zero (for perfect balance) by connecting a 10 kΩ potentiometer between the terminals 1 and 5 marked "off-set null". The middle terminal of the potentiometer is connected to as shown in figure.

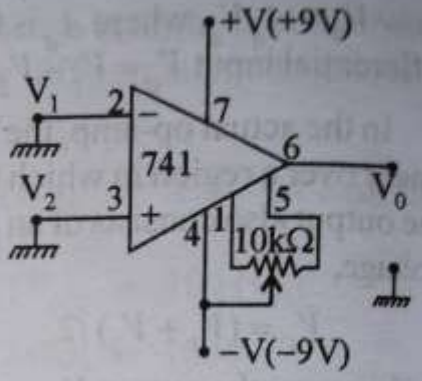


Fig. 196 *Off-set null arrangement*

Now, V_1 and V_2 made zero, by earth-connecting terminals 2 and 3. The output voltage is noted with respect to the ground by using a multimeter.

The 10 kΩ potentimeter is adjusted to get zero output voltage. The adjustment is known as "off-set null" adjustment and it must be preserved while using the op-amp in any circuit.

The input off-set voltage is defined as the voltage that must be applied between the two input terminals of an op-amp to null the output.

The important technical parameters of IC 741 are given below:

Supply voltage	:	$\pm V_{CC} = \pm 5$ to 18 V
Output resistance	:	$R_o = 2M\Omega$
Input resistance	:	$R_{in} = 75\Omega$
Voltage gain	:	$A_V = 200,000$ (106 dB)
Small signal band width	:	1 MHz
Power consumption	:	50 – 85 mW
Output short-circuit current	:	25 mA
Slew rate	:	0.5 V /μs

Bandwidth : Frequency response of amplifier

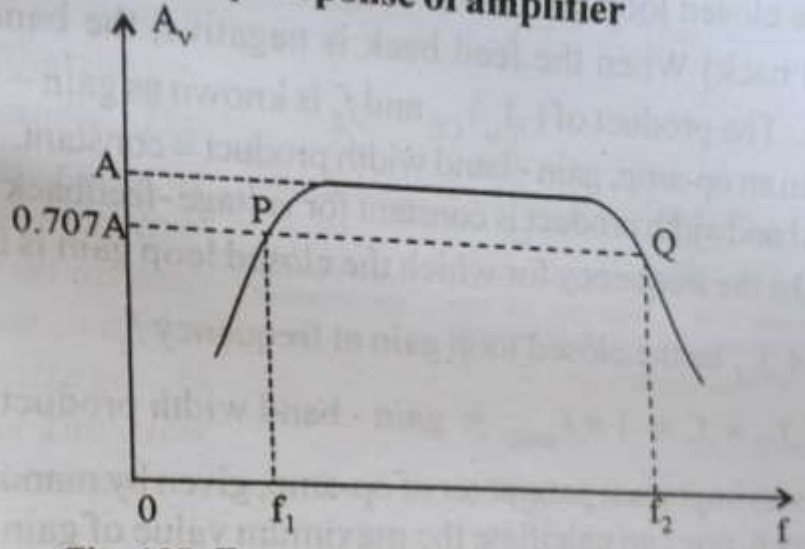


Fig . 197 *Frequency response of transistor amplifier.*

The gain of an amplifier is a function of frequency of the imput signal. The variation of gain with frequency is shown in the graph, known as the frequency response graph. At low frequencies, the gain increases with the frequency. At mid-frequency range, the gain remains constant. At high frequencies the gain is found to decrease with increase of frequency.

The point P on the graph corresponds to the gain = 0.707 times the maximum gain A, The frequency at this point is known as the *lower cut-off frequency* f_1. Similarly, the point Q corresponds to the gain = 0.707 times the maximum gain A on the higher frequency side. The frequency at this point is known as the *upper cut-off frequency*. The band of frequencies between f_1 and f_2 is known as the bandwidth (β) of the amplifier response i.e., $\beta = (f_2 - f_1)$.

For an op amp, the lower cut-off frequency $f_1 = 0$.

$\therefore$ band width $= f_2$ hertz

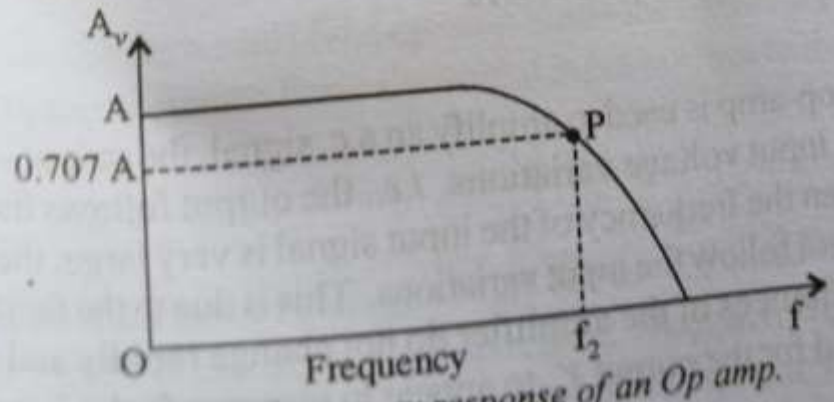


Fig. 198 *Frequency response of an Op amp.*

Let the closed loop gain of op-amp be $(A_v)_{CL}$ (closed loop means: with feed back) When the feed back is negative, the band width f_2 increases. The product of $(A_v)_{CL}$ and f_2 is known as gain – bandwidth product. In an op-amp, gain - band width product = constant. ie, The op-amp gain bandwidth product is constant for voltage -feedback amplifiers. Let f_{unity} be the frequency for which the closed loop gain is unity.

Let $(A_v)_{CL}$ be the closed loop gain at frequency f_2.

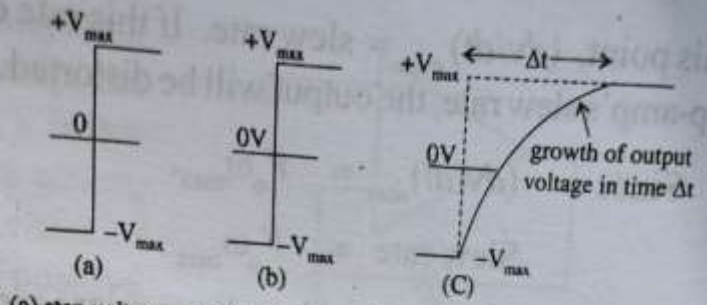
Then, $(A_v)_{CL} \times f_2 = 1 \times f_{unity}$ = gain - band width product

This is an important parameter of op-amp, given by manufacturer. If this is known, one can calculate the maximum value of gain $(A_v)_{CL}$ at a given value of frequency f_2; and also one can find f_2 for a given value of gain $(A_v)_{CL}$

Slew rate

When an op-amp is used to amplify an a.c. signal, the output varies as rapidly as the input voltage variations. *i.e.*, the output follows the input. However, when the frequency of the input signal is very large, the output variations do not follow the input variations. This is due to the fact that the internal capacitances of the amplifier do not change rapidly and a finite time is required for the output V_o to appear in response to the input.

So, there is upper limit to the frequency of the a.c. that the op-amp can handle. *The maximum rate of change of the output voltageof an op-amp in response to a step input voltage is known as the slew rate of the op-amp. The unit of slew rte is volts per microsecond (V/ μs).*



(a) step voltage input to op amp

(b) ideal output of op amp for step input (slew rate is infinity)

(C) Actual output response of op amp to step voltage input due to slew rate

Fig. 199 Slew rate

$$\text{Slew rate} = \frac{\Delta V_{out}}{\Delta t}$$

Thus, the slew rate sets a limit to the frequency of the input signal that the op-amp can handle. If the input signal has greater frequency than this limit, the output wave form will be distorted. For example, a square wave input may be distorted into a triangle wave in the output of the op-amp.

Open-loop operation

An op-amp can be used with or without external feedback. While using it without feedback, the operation is known as open loop operation. In this case, a very small signal (of the order of microvolt) at the input produces a large output (of the order of volt). The internal gain of the op-amp without external feedback is known as the open-loop gain, A_v. The open loop mode is often used for comparison of two signals (*i.e.*, as comparator).

Closed-loop operation: Positive and Negative feed back

In most cases, the op-amps are used with a feedback i.e., a portion of the output is feedback to the input. If the feedback from the output is

applied to the non-inverting input (+) terminal of the op-amp, the feedback is positive (Fig.). In this case, due to regenerative action, the output quickly increases to saturation. This type of positive regenerative feed back circuit is used in oscillators and logic gates.

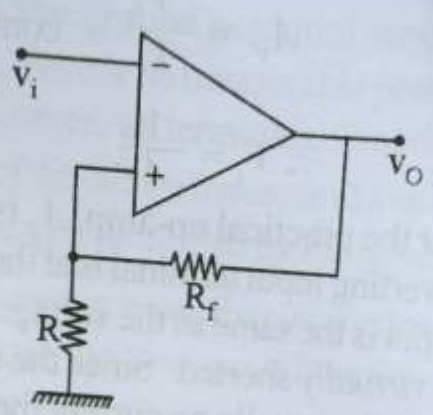


Fig. 200 *Positive feed back in op-amp.*

If the feed back is applied to the inverting input (–) terminal, the feed back is negative (Fig.). In this case, the gain of the amplifier system (A) is independent of op-amp characteristics but it depends on the feed back components (such as R_f) and hence the gain can be controlled. This type of feedback is used for amplification purpose.

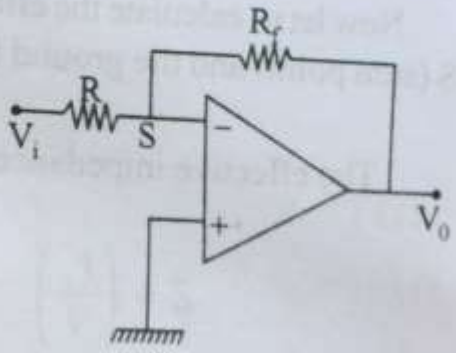
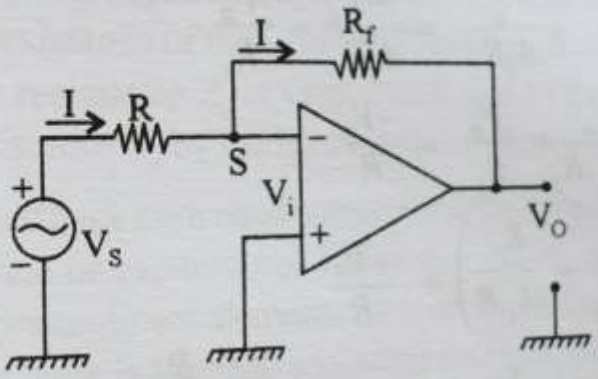


Fig. 201

Inverting operational amplifier



$R = 1\ k\Omega$

$R_f = 10\ k\Omega$

$A = -10$

Fig. 203 *Inverting operational amplifier.*

The inverting operational amplifier circuit is shown in the figure. A voltage source V_i (a.c or d.c) is connected to the inverting terminal of the op-amp through the resistance R. A negative feed back is given by connecting a resistance R_f between the output and the inverting input terminals. Nagative feed back means the returning signal through R_f has a phase that opposes the input signal. The feed back, in the case, is voltage shunt feed back.

V_i be the differential input voltage

voltage shunt feed back.

Let V_s be the source voltage, V_i be the differential input voltage (voltage at S) and V_o be the output voltage. By the virtual ground property of the op-amp circuit,

current through R = current through R_f

$$\frac{(V_s - V_i)}{R} = \frac{(V_i - V_o)}{R_f} \quad \ldots\ldots\ldots\ldots (1)$$

By definition of internal gain $A_V = \frac{-V_o}{V_i}$ (inverting input)

$$V_i = \frac{-V_o}{A_V}$$

Putting this in equation (1),

$$\frac{V_s - (-V_o/A_V)}{R} = \frac{(-V_o/A_V) - V_o}{R_f}$$

$$\frac{V_s}{R} + \frac{V_o}{A_V R} = \frac{-V_o}{A_V R_f} - \frac{V_o}{R_f}$$

$$\therefore \frac{V_o}{A_V R} + \frac{V_o}{A_V R_f} + \frac{V_o}{R_f} = \frac{-V_s}{R}$$

$$\frac{V_o}{R_f}\left(1 + \frac{1}{A_V} + \frac{R_f}{A_V R}\right) = \frac{-V_s}{R}$$

Since A_V is very large, $\frac{1}{A_V} < 1$ and $\frac{R_f}{A_V R} < 1$

$$\therefore \frac{V_o}{R_f} = \frac{-V_s}{R}$$

$$\therefore \text{Output voltage } V_o = -\left(\frac{R_f}{R}\right) V_s$$

$$\therefore \frac{V_o}{V_S} = -\left(\frac{R_f}{R}\right)$$

The gain of the amplifier with feed back is $A = \frac{V_o}{V_S}$

$$\therefore A = -\left(\frac{R_f}{R}\right)$$

(For example, if $R_f = 10\ \text{M}\Omega$ and $R = 1\text{M}\Omega$, A = −10. When the input voltage $V_s = 0.5\ V$, the output $V_o = -5\text{V}$).

Thus the closed loop gain of the amplifier depends on the feed back resistance R_f and the resistance R in the input circuit. By suitably changing the values of R_f and R, the desired gain can be obtained. Thus the feed back circuit elements decide the amplification character of the device.

The negative sign in the above expression shows that the output is inverted with respect to the input i.e., there is a phase reversal of 180° in the output. The output is stable due to the negative feed back.

current through R flows through R_f

The inverting operational amplifier circuit is *popular* for the following reasons:

1. It allows us to set up precise value of input impedance as well as voltage gain, as we desire. For example, if it is desired to set up an amplifier with input impedance 2 kΩ and gain 100, one can keep $R = 2\text{k}\Omega$ and $R_f = 200\ \text{k}\Omega$.

2. By virtual ground property, current through $R = (V_S / R)$, and current through R = current through R_f. The value of current through R_f is independent of the value of R_f. Whatever be the load resistance in R_f the same current (V_S / R) is driven through it by the op-amp. Thus the inverting amplifier circuit acts as a current source, sending constant output current $I_{out} = (V_S / R)$ through the load.

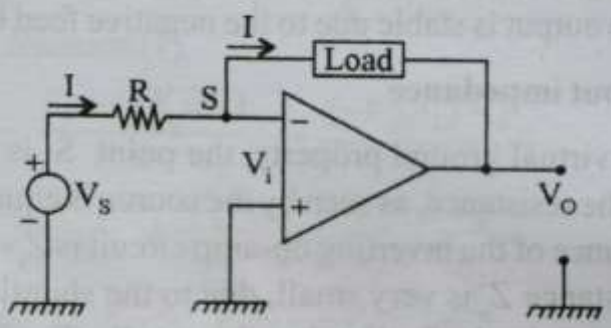


Fig. 204

3. Gain-bandwidth product

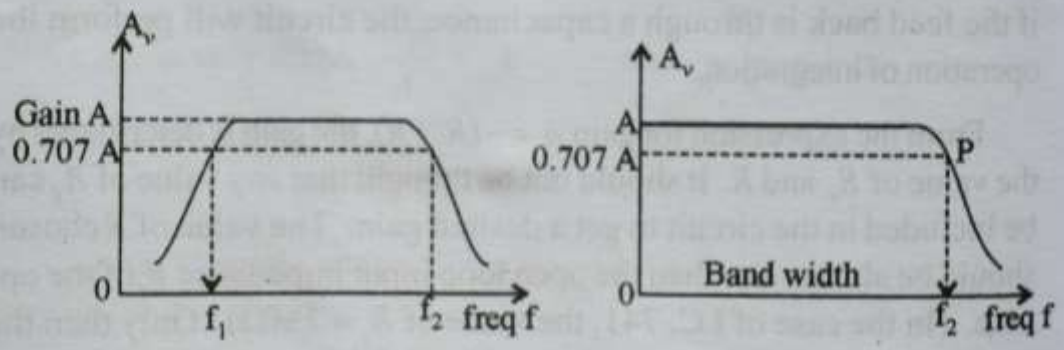


Fig. 205 *i.e., Bandwidth* = $(f_2 - f_1)$.

Bandwidth of an amplifier is the difference between the frequencies of upper cut-off and lower cut-off frequencies (fig. 180).

i.e., Bandwidth $= (f_2 - f_1)$.

Non-inverting operational amplifier

If an output which is in phase with the input is required, we make use of the non-inverting operational amplifier circuit. Figure shows an op-amp used as non-inverting amplifier. The input signal is applied to the non inverting input terminal (+) and the feed back is applied to the inverting input terminal (–) through R_f. A resistance R is connected to the ground from the inverting terminal. The resistors R_f and R form the feed back voltage divider circuit. The feed back is negative.

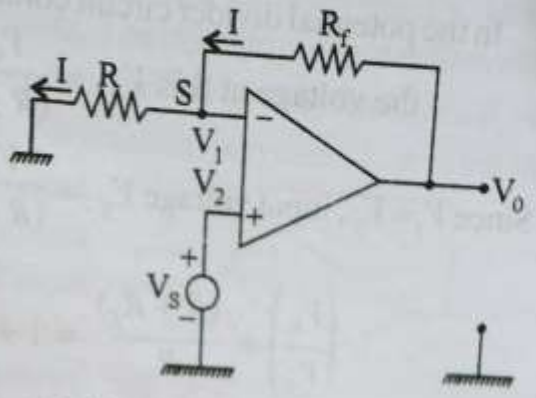


Fig. 215 *Non-inverting operational amplifier.*

To find the voltage gain, the following assumptions are made:

(i) The input impedance $= \infty$

i.e., no current flows in either of the two input terminals.

(ii) The open loop gain of the op-amp $A_v = -\infty$ *i.e.*, the potential of the two input terminals are equal. This can be seen from the following.

$$V_o = A_V(V_1 - V_2)$$

$$\therefore V_o = A_V(V_1 - V_S)$$

$$\therefore (V_1 - V_S) = \frac{V_o}{A_V}$$

Since $A_V = -\infty$, $V_1 - V_S = 0$ for finite output.

$$\therefore V_1 = V_S$$

To calculate the voltage gain

In the potential divider circuit containing the resistance R_f and R,

the voltage at S is $V_1 = \frac{V_o . R}{(R + R_f)}$

Since $V_1 = V_S$, input voltage $V_S = \frac{V_o . R}{(R + R_f)}$

$$\left(\frac{V_o}{V_S}\right) = \frac{(R + R_f)}{R} = 1 + \frac{R_f}{R} \qquad \frac{V_o}{V_S} = A$$

$$\therefore \text{Voltage gain } A = 1 + \left(\frac{R_f}{R}\right)$$

Thus, the closed loop voltage gain of the amplifier depends only on the ratio of the feed back resistors. The gain is not affected due to replacement of the op-amp or due to temperature change, *i.e.*, the closed loop gain has a rock-solid value. An a.c. output signal will be in phase with the input signal. A d.c. input signal will create amplified d.c. output signal of the same polarity.

The input impedance of the amplifier is equal to the input impedance of the non-inverting terminal of the op-amp, *i.e.*, $Z_i = \infty$. The output impedance $Z_o = 0$. The product of gain and the upper cut-off frequency (called gain-bandwidth product) is constant *i.e.*, by decreasing the closed-loop gain, the bandwidth of the frequency response of the circuit can be increased.

Voltage follower (Unity gain buffer)

Consider a non-inverting operational amplifier circuit, with feed back resistor R_f and R. The closed loop voltage gain is given by

$$A = 1 + \frac{R_f}{R}$$

When $R_f = 0$ (short circuit) and $R = \infty$ (open circuit).

the gain is $A = 1$

i.e., output voltage = input voltage both in magnitude and phase.

The output voltage follows the input voltage variation exactly. Hence, the circuit is called a voltage follower. The input impedance of the voltage follower is equal to the input impedance of the op-amp itself, i.e., $Z_i \to \infty$ The output impedance Z_o is zero for practical purposes. Due to the high input impedance and the low output impedance, the voltage follower circuit isolates the signal sources at the input side and the load at the output side. This prevents the undesired interactions between the load and the source (the loading effect is prevented). The above said isolation is known as the *buffer action*. Thus the voltage follower acts as a *unity gain buffer*.

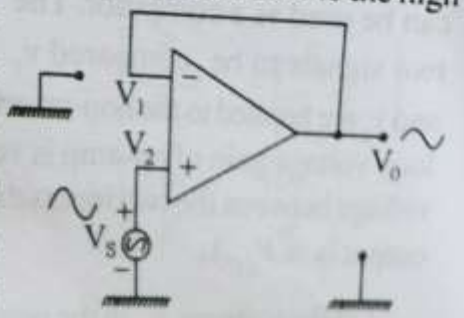


Fig. 216 *Voltage follower.*

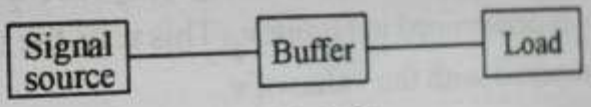


Fig. 217

Uses

(i) Buffer amplifiers are used to isolate signal sources from any loading effects.

(ii) They are also useful when working with signal sources that have high internal impedances. i.e., they are used as *impedance matching device*. Thus, the unity gain buffer can function as an impedance transformer.

...mp circuits ...d to solve second order

Summing amplifier (Adder circuit)

Figure shows an operational amplifer used for summing two or more a.c. or d.c. voltages. The input sources of voltages V_1, V_2 and V_3 are connected to the inverting input terminal through the resistances R_1, R_2 and R_3 respectively. The non-inverting terminal is earth-connected. The output is fed back to the inverting input terminal through the resistance R_f i.e., the feed back is negative.

Due to the negative feed back, the summing point S is at the virtual ground. Since the input impedance of the op-amp $R_i = \infty$, the current entering S through R_1, R_2 and R_3 is equal to the current leaving S but flowing through R_f

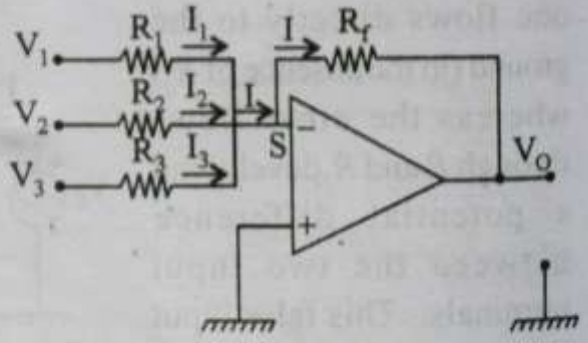


Fig. 207 *Summing amplifier.*

i.e., $I_1 + I_2 + I_3 = I.$

Since the summing point S is at zero potential,

$$\frac{(V_1 - 0)}{R_1} + \frac{(V_2 - 0)}{R_2} + \frac{(V_3 - 0)}{R_3} = \frac{(0 - V_o)}{R_f}$$

$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = \frac{-V_o}{R_f}$$

$$V_o = -R_f \left(\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} \right)$$

If $R_1 = R_2 = R_3 = R$, the output voltage $V_o = -\frac{R_f}{R}(V_1 + V_2 + V_3)$

Thus, the output voltage is proportional to the sum of the input voltages

If $R_f = R$, $V_o = -(V_1 + V_2 + V_3)$

Then the output will be the inverted sum of the input voltages.

Uses

(i) The summing amplifiers are used as mixers for mixing different signal voltages. When audio recording is made, the output signals from different microphones are to be mixed to get the final signal. This is done using a summing amplifier.

(ii) In getting the final signal, all the microphone signals are not weighted equally *i.e.*, they are multiplied by different constant values before they are combined, *i.e.*, individual signals can be amplified to any desired values and then they can be summed up by this circuit. The over - all gain can be adjusted by changing R_f in the adder circuit.

(iii) Since the inverting input is at the virtual ground, there is no intervention between the inputs. *i.e.*, the circuit prevents one input signal from appearing at the other input (the current due to one source does not flow through any other source).

...thematical average

through any other source).

(iv) A summing amplifier can be made to give the mathematical average of the input voltages. This is done by setting the resitance ratio as

$\left(\frac{R_f}{R}\right) = \frac{1}{n}$ where n is the number of inputs. In that case,

the gain $\frac{V_o}{V_i} = -\left(\frac{R_f}{R}\right)$

$\therefore \frac{V_o}{\text{total input}} = -\frac{1}{n}$

$$V_o = -\frac{(V_1 + V_2 + V_3)}{n}$$

Subtracting amplifier (difference amplifier)

An op-amp can be used in subtracting mode. Figure shows the circuit that gives an output proportional to the difference between two input voltages.

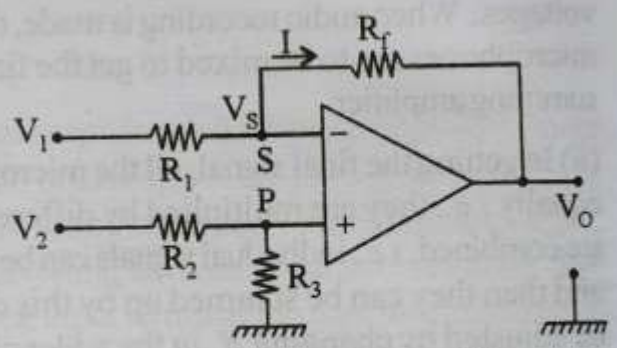


Fig. 208 *Subtracting amplifier.*

V_1 is the voltage of one input source, connected to the inverting terminal through R_1, V_2 is the voltage of the other source connected to the non-inverting terminal through the resistance R_2. R_f is the feed back resistance connected between the output and the summing point S. A resistance R_3 is connected between the non-inverting terminal and the ground to provide a path for current from the source V_2. The resistance R_2 and R_3 form a potential divider arrangement. Hence, the voltage at P is given by

$$V_P = \frac{V_2 . R_3}{R_2 + R_3}$$

If $R_2 = R_3$ we have $V_P = \frac{V_2}{2}$ ..... (1)

Due to negative feed back, the voltage at S and P are the same

i.e., $V_S = V_P$

The voltage at S is given by $V_S = \frac{V_2}{2}$ ..... (1)

The input impedance of the op-amp is infinity. Hence,

Current through R_1 = current through R_f

$$\frac{V_1 - V_S}{R_1} = \frac{V_S - V_o}{R_f}$$

$$\frac{V_1 - (V_2/2)}{R_1} = \frac{(V_2/2) - V_o}{R_f}$$

If $R_1 = R_f$, $\quad V_1 - \frac{V_2}{2} = \frac{V_2}{2} - V_o$

$$V_o = (V_2 - V_1)$$

Thus, the output voltage is equal to the difference between the input voltages.

Op-amp as integrator

A circuit that performs the operation of integration is shown in the figure.

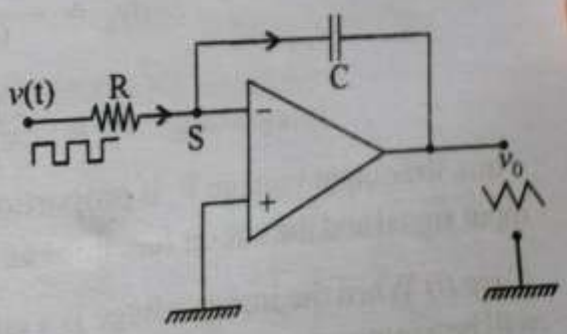


Fig. 209 *Op-amp as integrator.*

The input signal source of voltage $v(t)$ is connected to the inverting input terminal through resistance R. The negative feed back is given using a capacitor C. The non inverting terminal is earth-connected. This makes the summing point S at zero potential.

Let $v(t)$ be the signal voltage (square wave) given as input, which drives a current through R. Due to the virtual ground at the summing point S, the capacitor's charging current is made constant (not exponential as other-wise).

Current through R = Current through C.

$$\frac{\upsilon(t) - 0}{R} = \frac{dQ}{dt} \qquad i = \left[\frac{dQ}{dt}\right]$$

$$\therefore \quad \frac{dQ}{dt} = \frac{\upsilon(t)}{dt} \qquad \ldots\ldots (1)$$

where Q is the charge on the capacitor at any instant. Let the capacitance of the capacitor $= C$.

Potential difference across the capacitor $= 0 - \upsilon_o = -\upsilon_o$

The charge developed on the capacitor $Q = (CV) = -C\upsilon_o$ at any instant t.

$$Q = -C v_o \qquad \therefore \frac{dQ}{dt} = -C\left(\frac{dv_o}{dt}\right)$$

Using this in equation (1), $\frac{v(t)}{R} = -C\frac{dv_o}{dt}$

$$\therefore \frac{dv_o}{dt} = \frac{-1}{CR} v(t)$$

$$\therefore dv_o = -\frac{-1}{CR} v(t).dt$$

$$\text{Integrating,} \quad v_o = \frac{-1}{CR} \int v(t).dt$$

Thus, the output voltage V_o is proportional to the integrated value of the input signal and the circuit functions as an integrator.

Case (i) When the input voltage is a constant $v(t) = V$, then the output will be a ramp:

$$v_o = \frac{-1}{CR}\int_o^t v\,dt \qquad v_o = \frac{-V}{CR}\int_o^t dt$$

$$v_o = \frac{-V}{CR}.t \qquad \ldots\ldots (2)$$

The output is found to decrease with time t,

By a separate arrangement, the capacitor is made to discharge after reaching a particular time, making $v_o = 0$. The process can be repeated. Such an integrator, producing a ramp output, can be used as a (time-

base) sweep circuit for a CRO and it is called a Miller integrator.

The slope of the sweep $= -V/CR$ (from equation 2). This gives the rate of change of output voltage. Hence the time-base can be varied by varying V, or the time constant value of $(1/CR)$. Linear ramps like this are used in digital voltmeters, oscilloscopes and many other applications such as analog computations. The integrator circuit is mostly used in analog computers, analog- to-digital converters and wave - shaping circuits.

Case (ii) When the input voltage is a square wave, the output will be a triangle wave. When the input is +5V, the output is a negative going ramp. It reaches –5 V at the end of the first pulse. The input and output waveforms are as shown in figure.

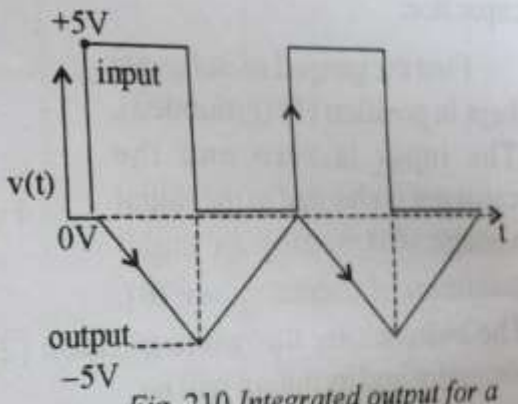


Fig. 210 Integrated output for a square wave input

The integrating circuits are used to solve differential equations in analog computers.

Op-amp as differentiator

A circuit that performs the operation of differentiation is shown in the figure .

The input signal source of voltage $v(t)$ is connected to the inverting input terminal through a capacitor C. The non-inverting input terminal is earth-connected. Negative feed back is given through a resistance, R.

Let $v(t)$ be the signal voltage given as the input, which drives varying current through the capacitance C. Due to the virtual ground at the summing point S,

current through C = current through R.

$$\left(\frac{dQ}{dt}\right) = \frac{0 - v_o}{dt} = -\frac{v_o}{R} \qquad \ldots\ldots\ldots\ldots (1)$$

But Q is the charge on the capacitor at any instant t. i.e., $Q = C.v(t)$. Using this in equation (1).

$$C \cdot \frac{dv(t)}{dt} = -\frac{v_o}{R}$$

$$\therefore \quad v_o = -CR \cdot \frac{dv(t)}{dt} \quad \text{(differentiator output)}$$

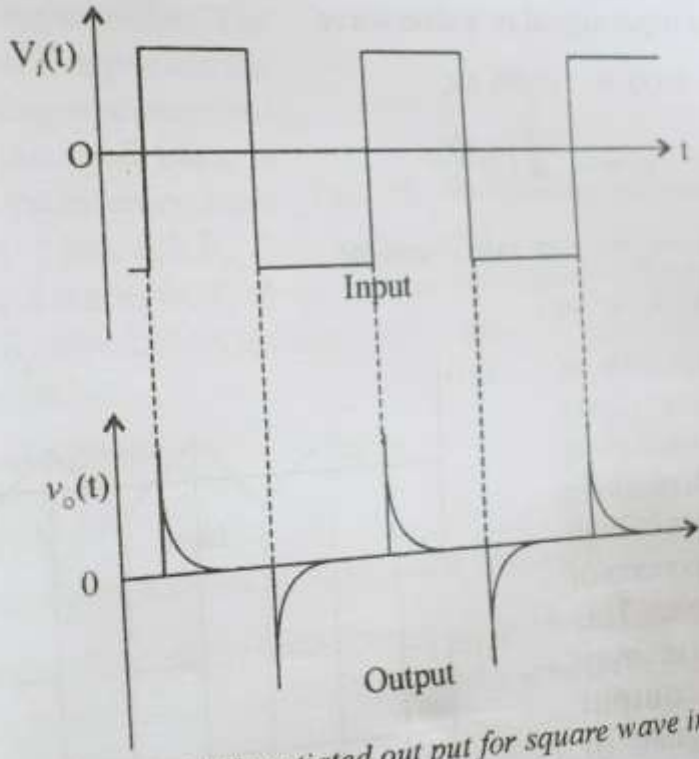


Fig. 213 *Differentiated out put for square wave input.*

The output is proportional to the time derivative of the input signal and the circuit functions as a differentiator, showing the amount of instantaneous variations of the input quantity. The quantity (CR) is the time constant of the circuit.

Case (i)

When the input signal is a square wave, the output contains sharp spikes, which are instantaneous variations of the input as in figure. The advantage of an op-amp differentiator over a simple RC differentiator

(passive) is that the output spikes are narrow and are coming from a low impedance source. This makes driving current large through load easier. The sharp pulses can be used as trigger pulses in circuits.

Case (ii)

When the input is a triangular wave (ramp), the output is a square wave.

Case (iii)

When the input signal is a sine wave

$$v(t) = a \sin \omega t,$$

$$v_o = - RC \frac{dv_i}{dt}$$

the output $v_o = -a\ \omega RC \cos \omega t$

i.e., $v_o \propto \omega$

Thus, the magnitude of the output increases linearly with increasing frequency. This results in the amplification of high frequency components of the amplifier noise. This amplified noise may obscure the output differentiated signal. To minimise the problem of *noise magni fication,* a small capacitor may be connected parallel to the feed back resistor to by-pass the high frequencies.

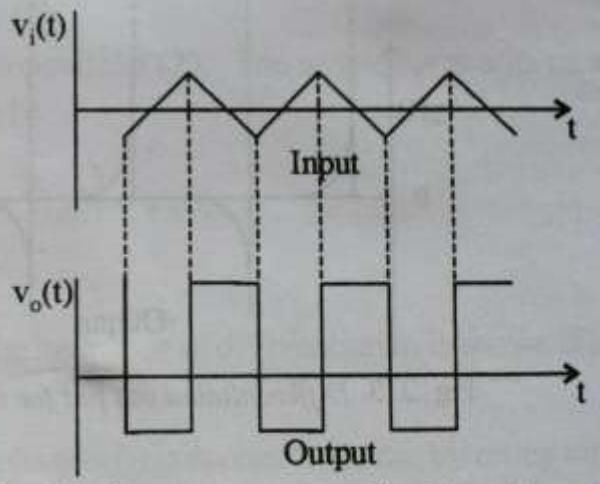


Fig. 214 *Square wave output for triaugular wave input of a op-amp differentiator.*

The differentiator circuits can be used to solve differential equation in analog computers. However, they are seldom used due to the noise magnification problem at high frequencies. The important application of op-amp differentiator is to produce a rectangular output from a ramp input.

Questions

1. What is an operational amplifier? Give its schematic symbol, equivalent circuit and a.c. analysis.
2. Write about bandwidth and slew rate of operational amplifier.
3. Write about frequency response of op-amp.
4. List out (i) ideal characteristic of op-amp and (ii) the applications of op-amp.
5. Giving neat circuit diagram, explain the working of opamp with negative feedback.
6. What are the applications of negative feed back op-amp?
7. Why are negative feedback amplifiers more popular?
8. Explain the concept of virtual ground in op-amp. How is virtual ground different from real ground point?
9. Describe, with a neat circuit diagram, the action of inverting amplifier with op-amp. Derive an expression for voltage gain of an inverting amplifier..
10. Write about input and output impedances of inverting amplifier with op-amp.
11. Describe, with circuit diagram, the working of non-inverting amplifier with op-amp. Derive an expression for its voltage gain.
12. Draw the circuit diagram of voltage follower with op-amp and explain its working. Show that the voltage gain of voltage follower is unity. Write one important application of voltage follower.
13. Draw the circuit diagram of summing amplifier using op-amp. Derive an expression for its output. Also describe how average of three voltages v_1, v_2 and v_3 can be obtained using summing amplifier.
14. Describe, giving relevant circuit diagram,
    (i) adder and (ii) subtractor using op-amp.

16. For square waves inputs explain how sharp spikes of signals could be obtained using electronic circuit. Give the circuit diagram and functioning of the electronic circuit using op-amp..

Objective type questions

1. An ideal op-amp has

   (a) infinite voltage gain (b) infinite input impedance

   (c) zero output impedance (d) all the above

2. Virtual ground is any point in a circuit that has

   (a) zero voltage and draws zero current

   (b) zero voltage and draws any amount of current

   (c) any amount of voltage and draws zero current

   (d) all the above.

3. When negative feedback is used, the gain-bandwidth product of an op-amp

   (a) increases (b) decreases

   (c) remains the same (d) fluctuates

4. In an integrator using op-amp, the feedback element is

   (a) resistor (b) capacitor

   (c) zener diode (d) voltage divider

5. In a differentiator using op-amp, the feedback element is a

   (a) resistor (b) capacitor

   (c) zener diode (d) voltage divider

6. When the input to a differentiator with op-amp is triangular wave form, the output is

   (a) a d.c. level (b) an inverted triangle

   (c) square waveform (d) first harmonic of input

(c) square waveform

7. In a summing amplifier using op-amp, the currents passing through resistors on the input side are such that

(a) they pass through all resistors equally

(b) they cancel each other at the virtual ground

(c) current in one branch does not affect the currents in other branches.

(d) all the above.

8. CMRR of an op-amp is the ratio

(a) $\frac{\text{differntial gain } (A_d)}{\text{common mode gain } (A_c)}$ (b) $\frac{\text{common mode gain } (A_c)}{\text{differential gain } (A_d)}$

(c) $A_d - A_c$ (d) $A_c - A_d$

9. Power bandwidth of an op-amp is equal to

(a) slew rate (b) $\frac{\text{slew rate}}{2\pi V_{max}}$

(c) $\frac{2\pi V_{max}}{\text{slew rate}}$ (c) $\frac{\text{Power}}{\text{band width}}$

10. The main purpose of using voltage follower is to have

(a) high voltage gain (b) low voltage gain

(c) unity gain (d) impedance matching

11. In an inverting op-amp circuit, the feedback resistor is increased four times. The current through that resistor will be

(a) increased four times (b) decreased one fourth

(c) the same as before (d) zero

12. Input off-set voltage of an op-amp is

(a) the output voltage, when the inputs are shorted.

(b) the output voltage, when the inputs are earthed

(c) the voltage to be applied between the two input to null the output voltage.

(d) the output voltage, without giving power supply to the op-amp.

13. The input impedance of an ideal op-amp is

(a) zero (b) infinity

(c) between zero and infinity (d) always negative

14. Sharp spikes of signals for trigging can be obtained with the help of op-amp

(a) adder (b) subtractor (c) differentiator (d) integrator

15. It is desirable that an amplifier circuit with op-amp has

(a) small differential gain (b) small common mode gain

(c) large differential gain (d) large common mode gain

16. The voltage gain of op-amp voltage follower is

(a) zero (b) infinity (c) one (d) less than one.

17. A certain op-amp has bias currents of 50 μA and 49.3 μA. The input off set current is

(a) 0.7 μA (b) 49.7 μA (c) 0.35A (d) none

18. The op-amp can amplify

(a) a.c. signals only (b) d.c. signals only

(c) both a.c. and d.c. signals (c) neither d.c. nor a.c. signals

Answers

1. (d)	2. (a)	3. (c)	4. (b)	5. (a)
6. (c)	7. (c)	8. (a)	9. (b)	10. (d)
11. (c)	12. (c)	13. (b)	14. (c)	15. (b)
16. (c)	17. (a)	18. (c)		